

ABSTRACT

A method includes a resin sealing step of placing, in a cavity 28 of a mold 20, a substrate 16 to which semiconductor elements 11 on which bumps 12 are arranged, a resin sealing step of supplying resin 35 to positions of the bumps 12 so that a resin layer 13 sealing the bumps 12 is formed, a protruding electrode exposing step of exposing at least ends of the bumps 12 sealed by the resin layer 13 so that ends of the bumps 12 are exposed from the resin layer 13, and a separating step of cutting the substrate 16 together with the resin layer 13 so that the semiconductor elements 11 are separated from each other.

図 1

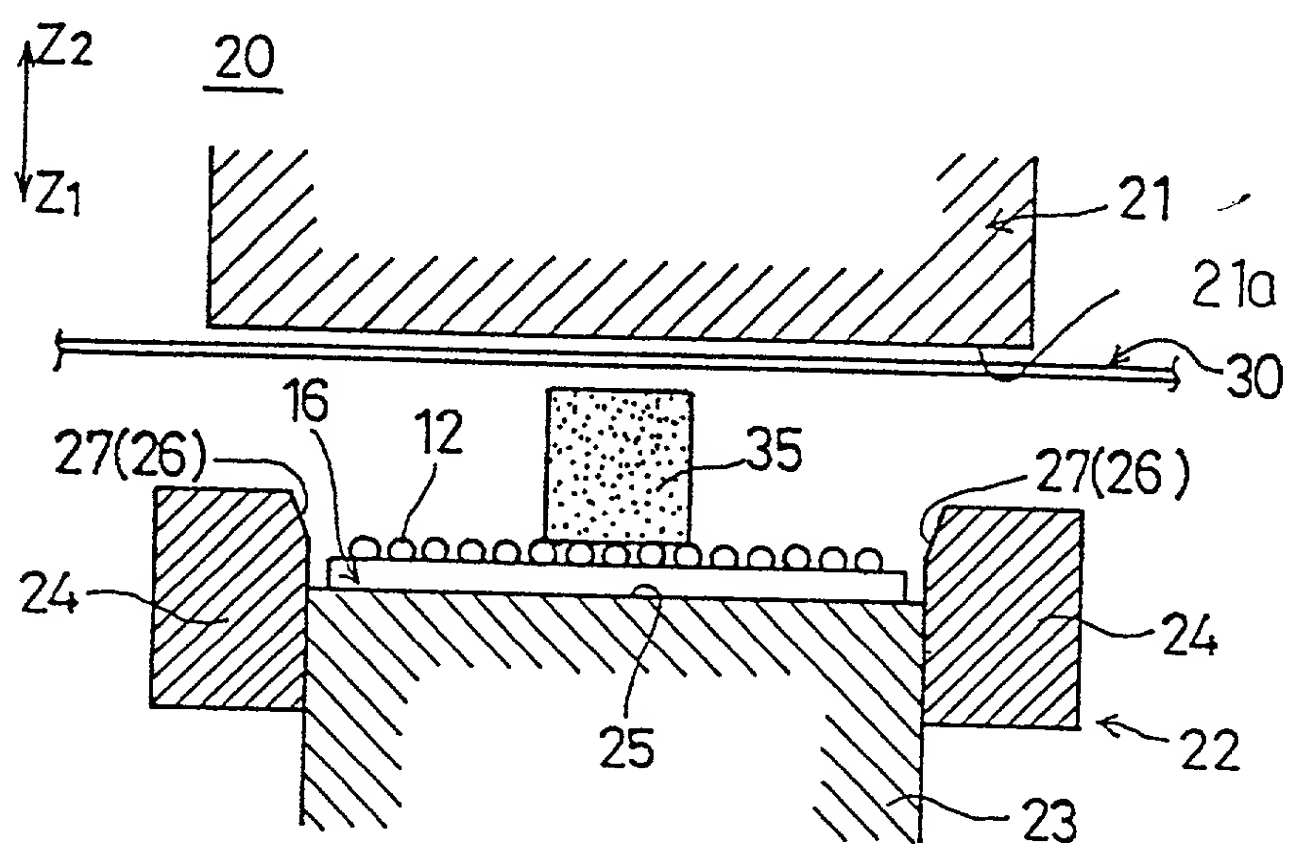


図 1 A

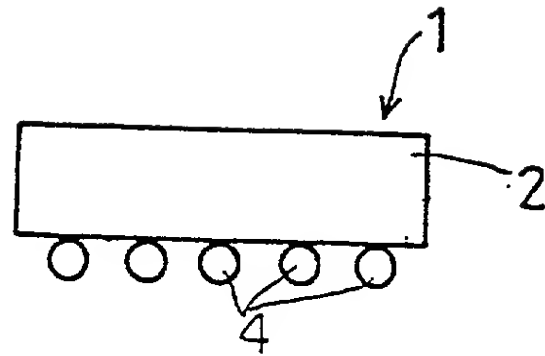


図 1 B

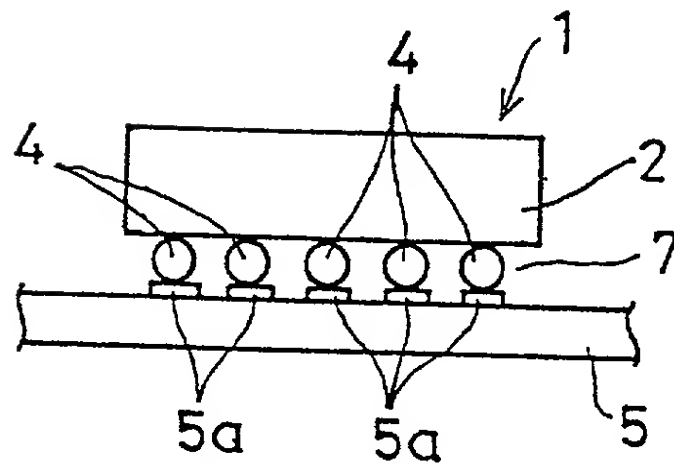


図 1 C

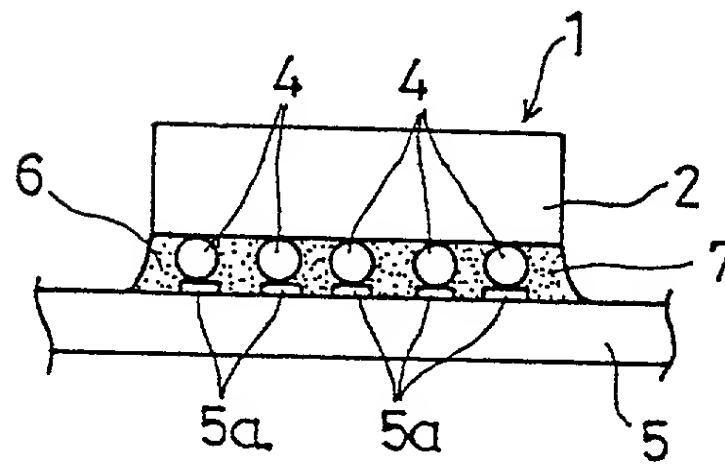


図 3

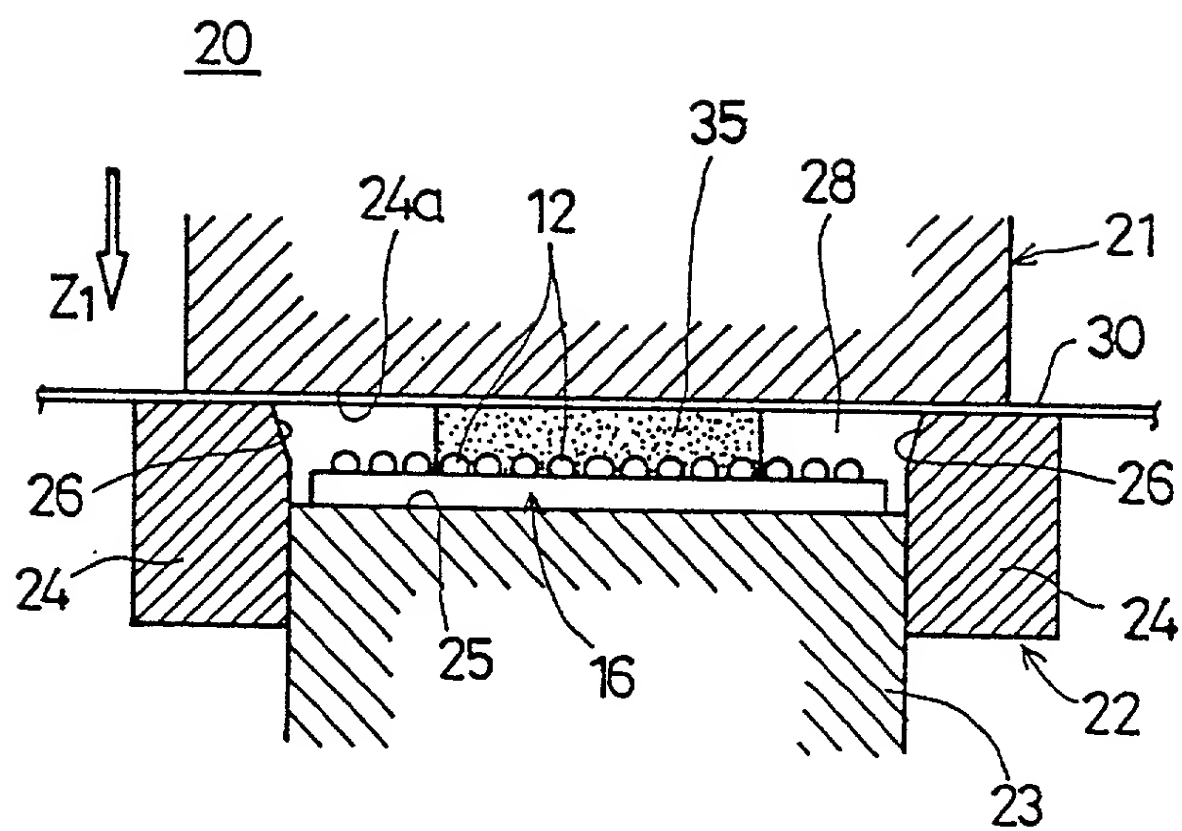
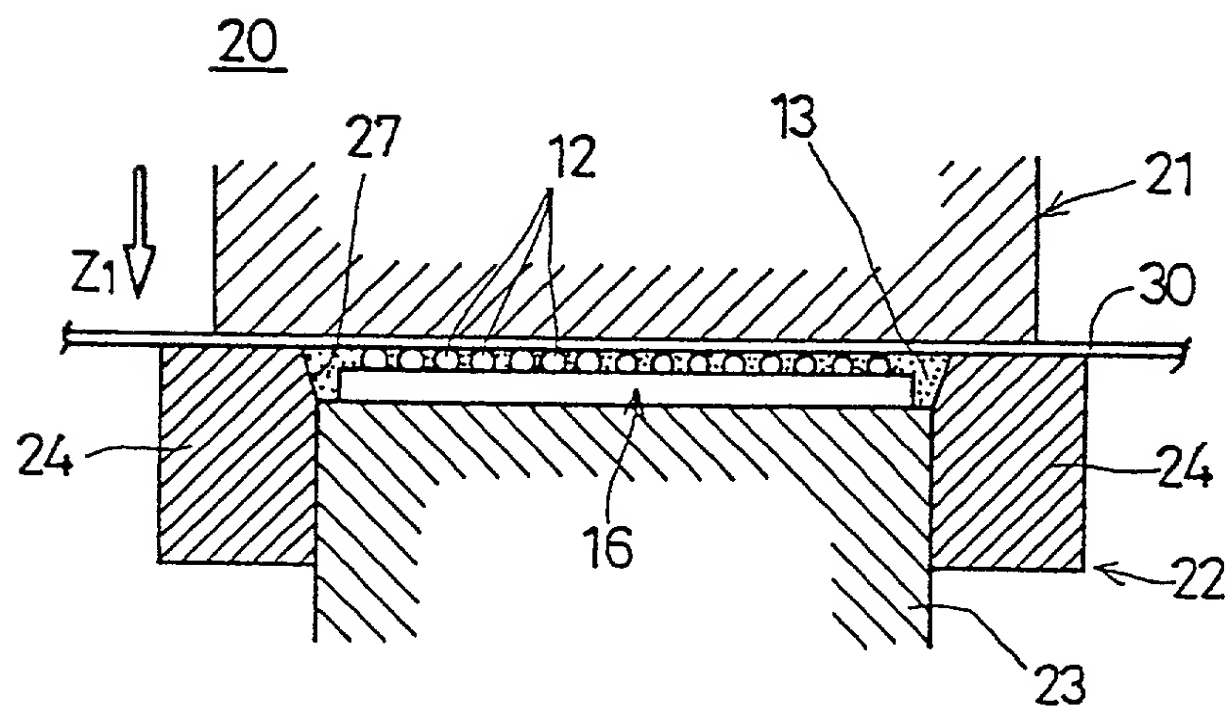
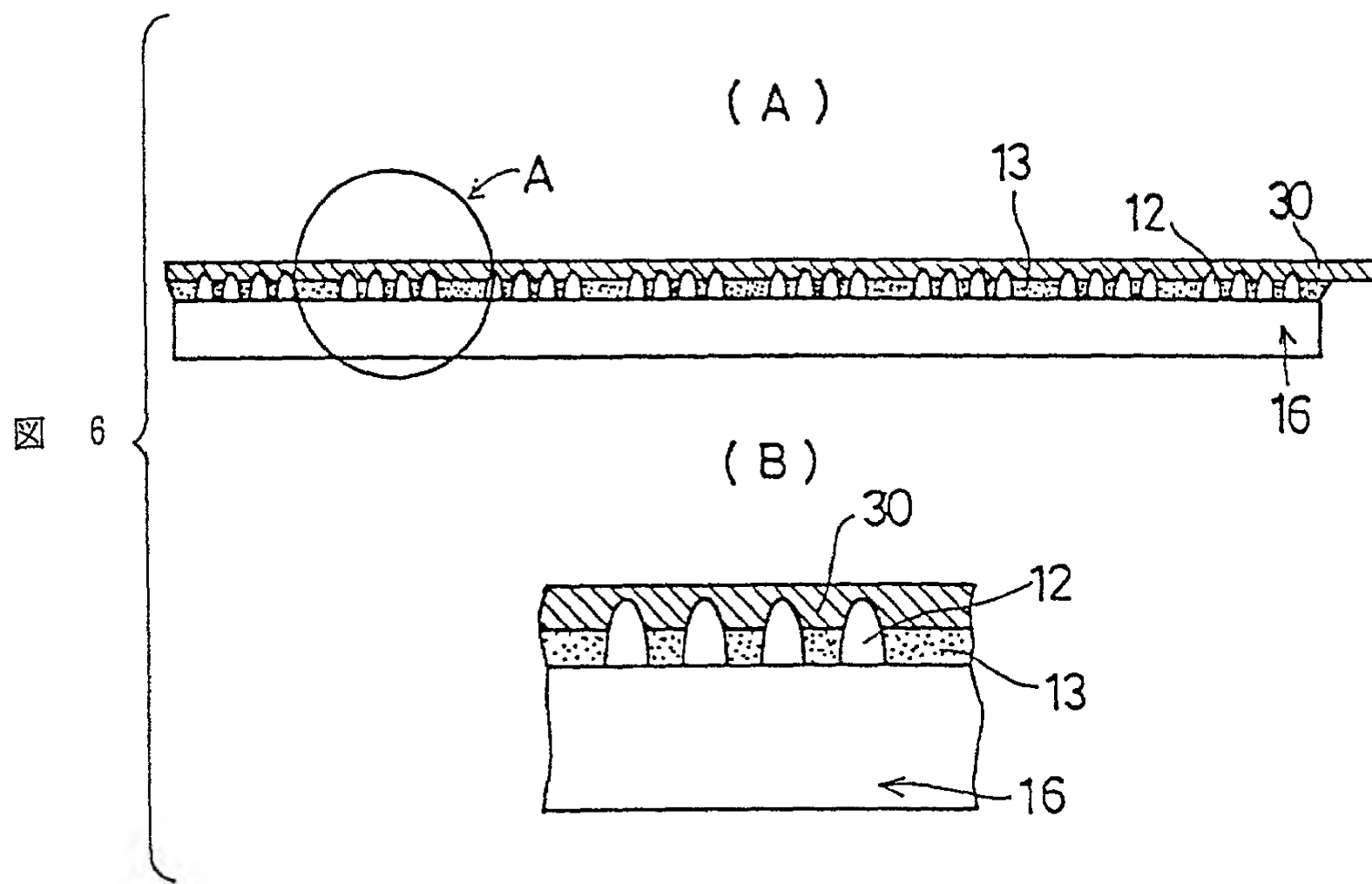
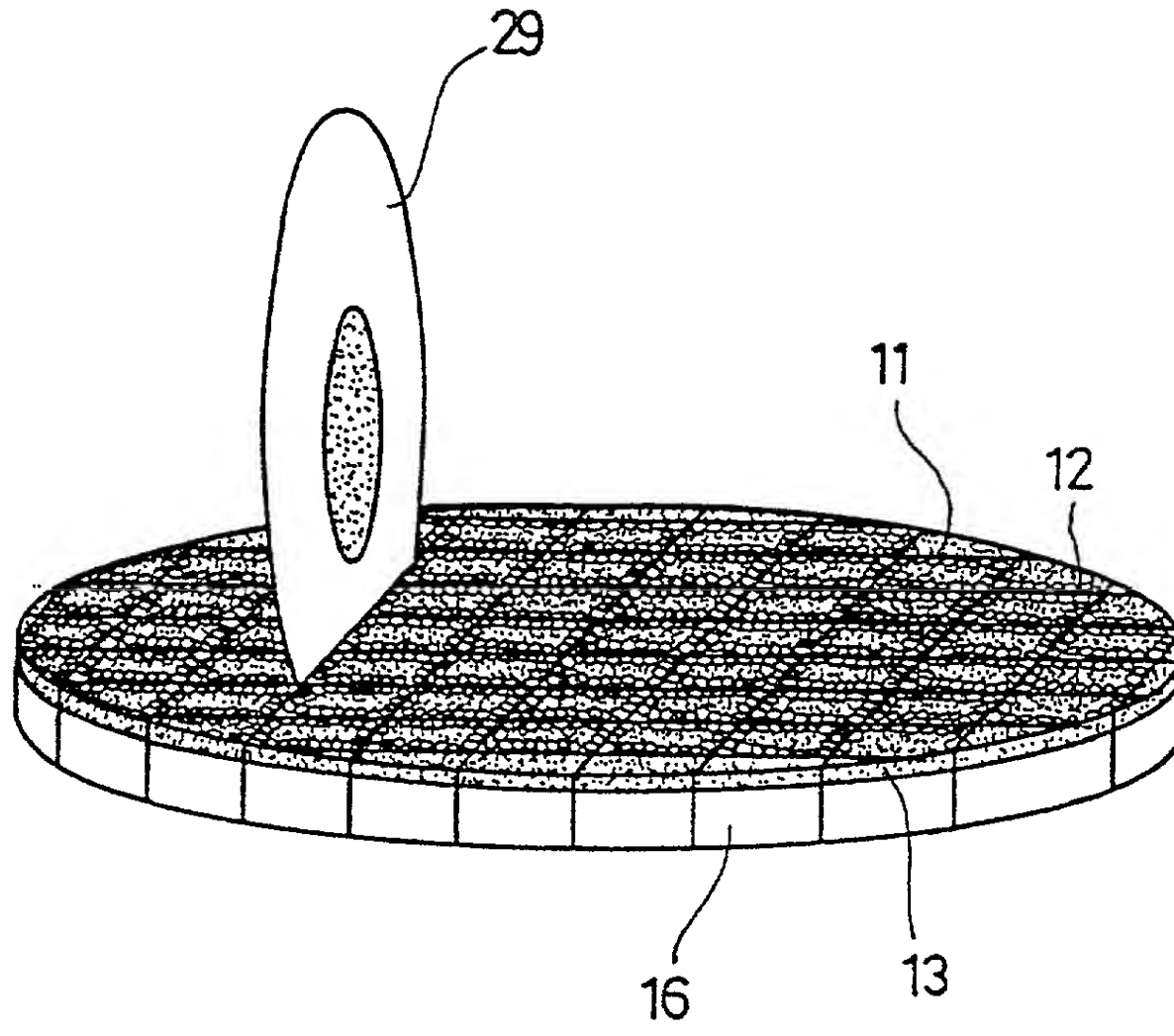


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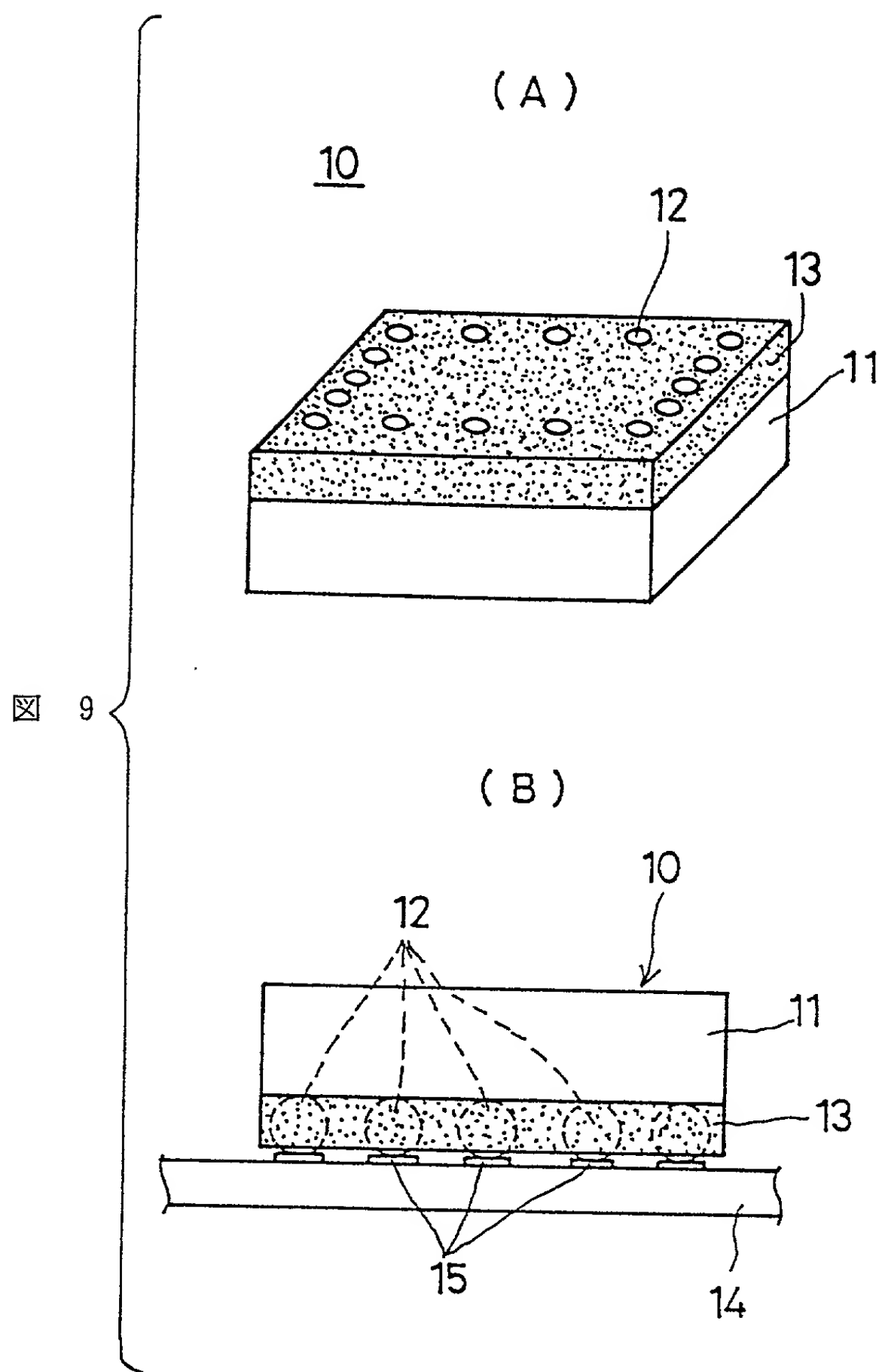




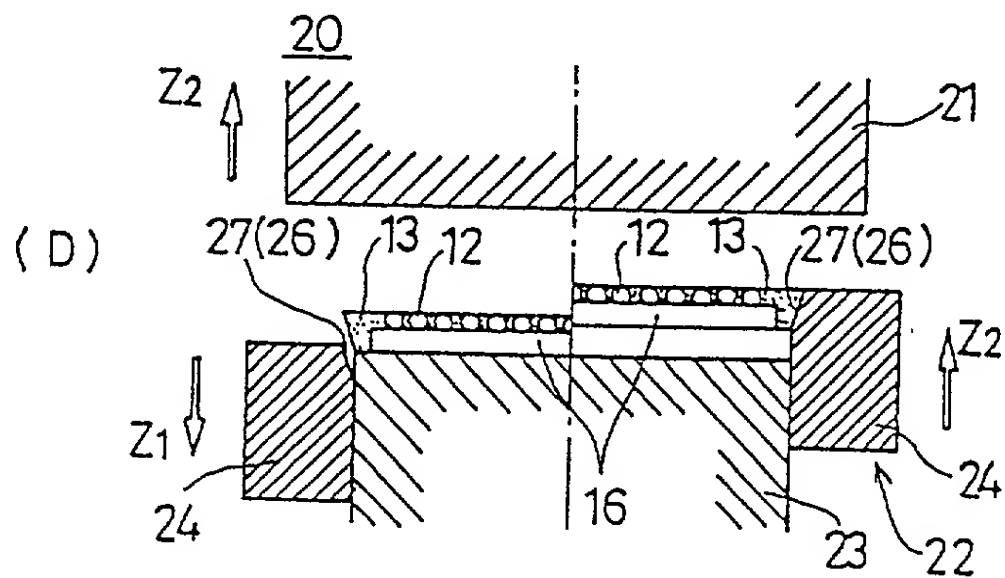
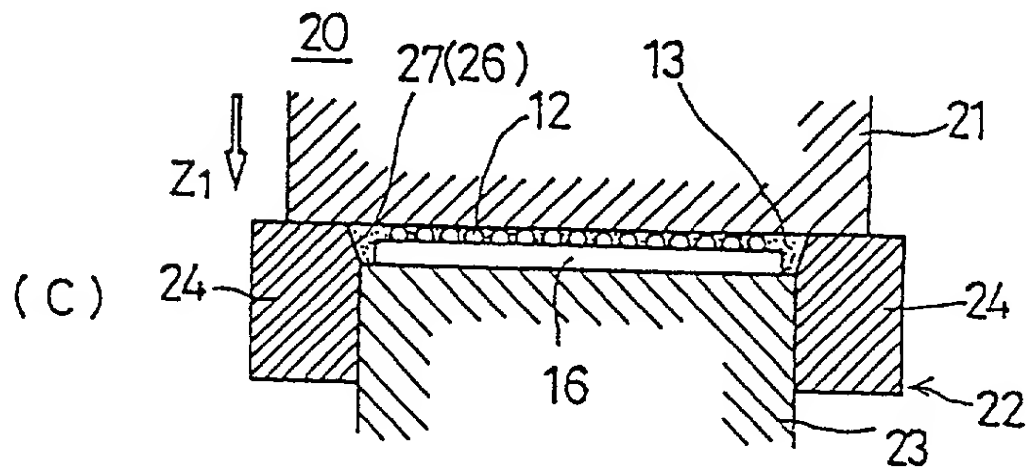
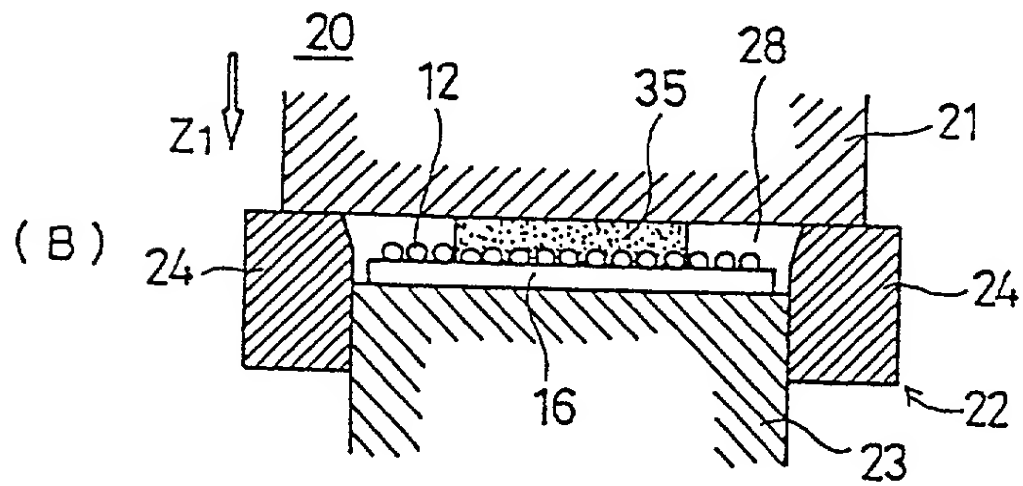
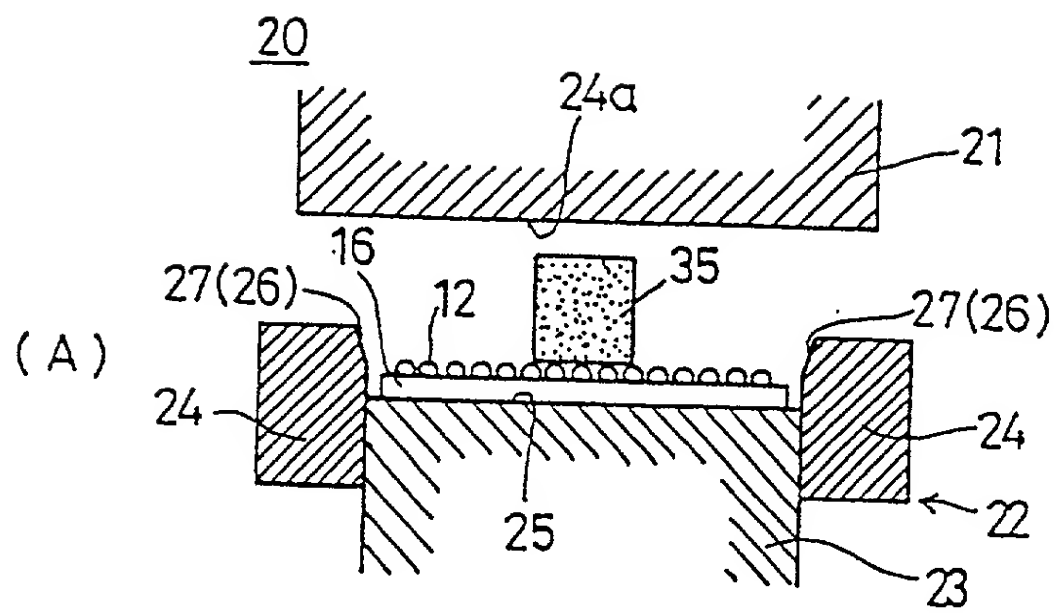
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9 10 11 12 13 14 15



11



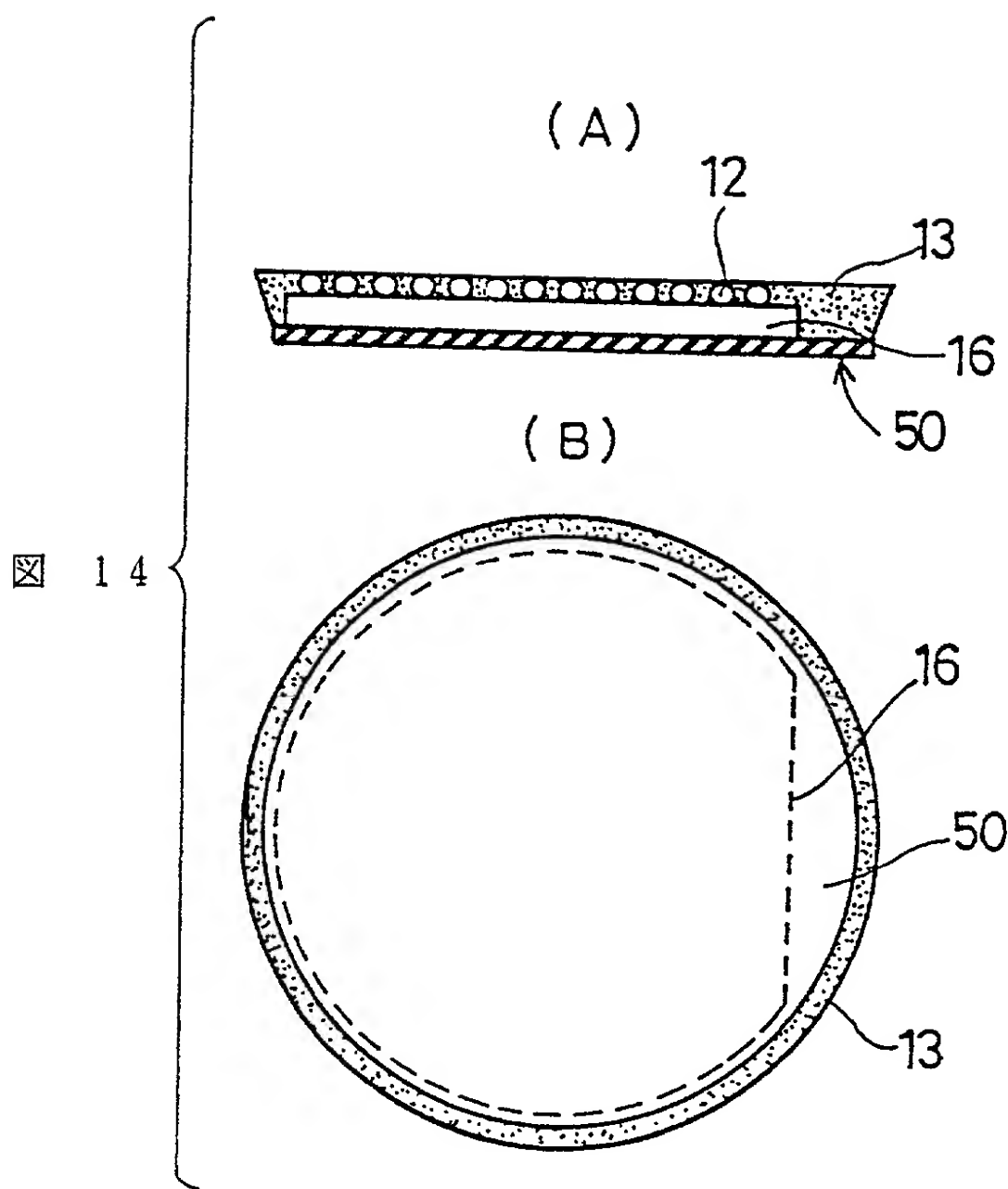
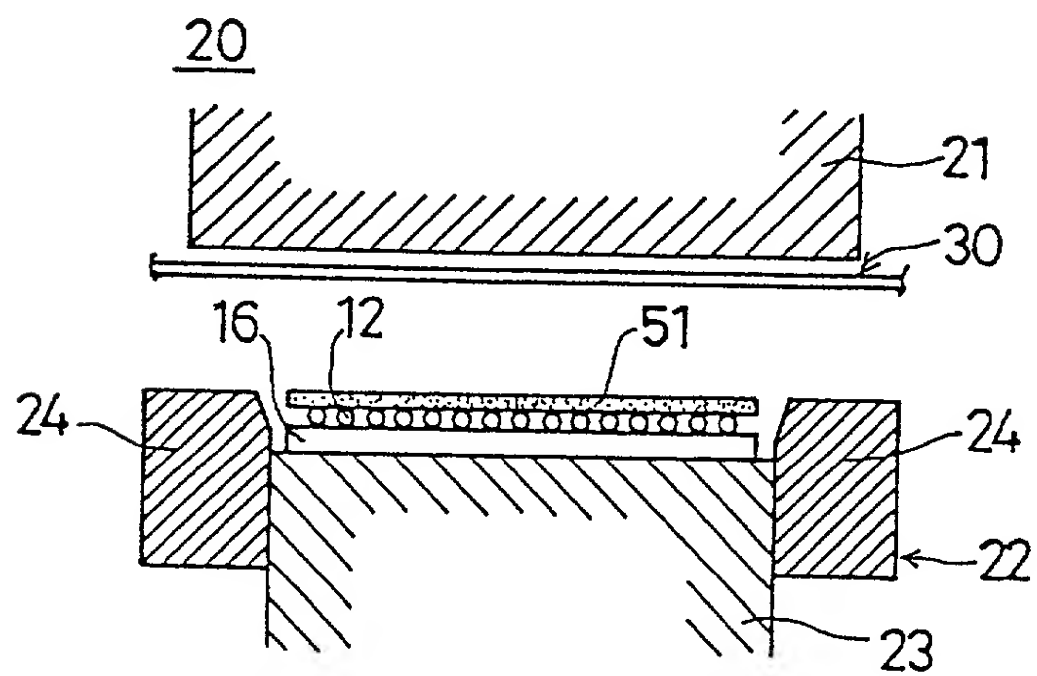
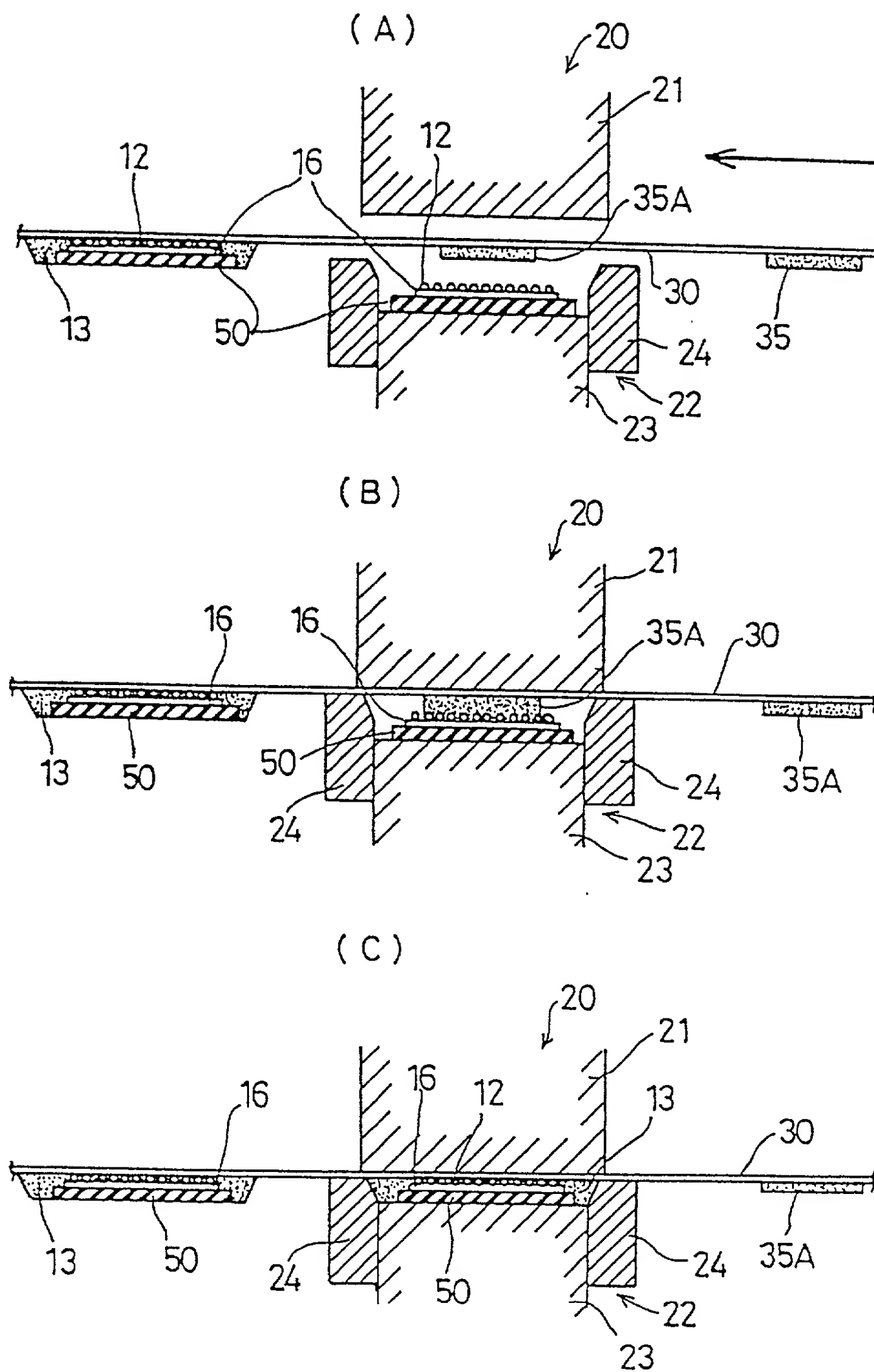
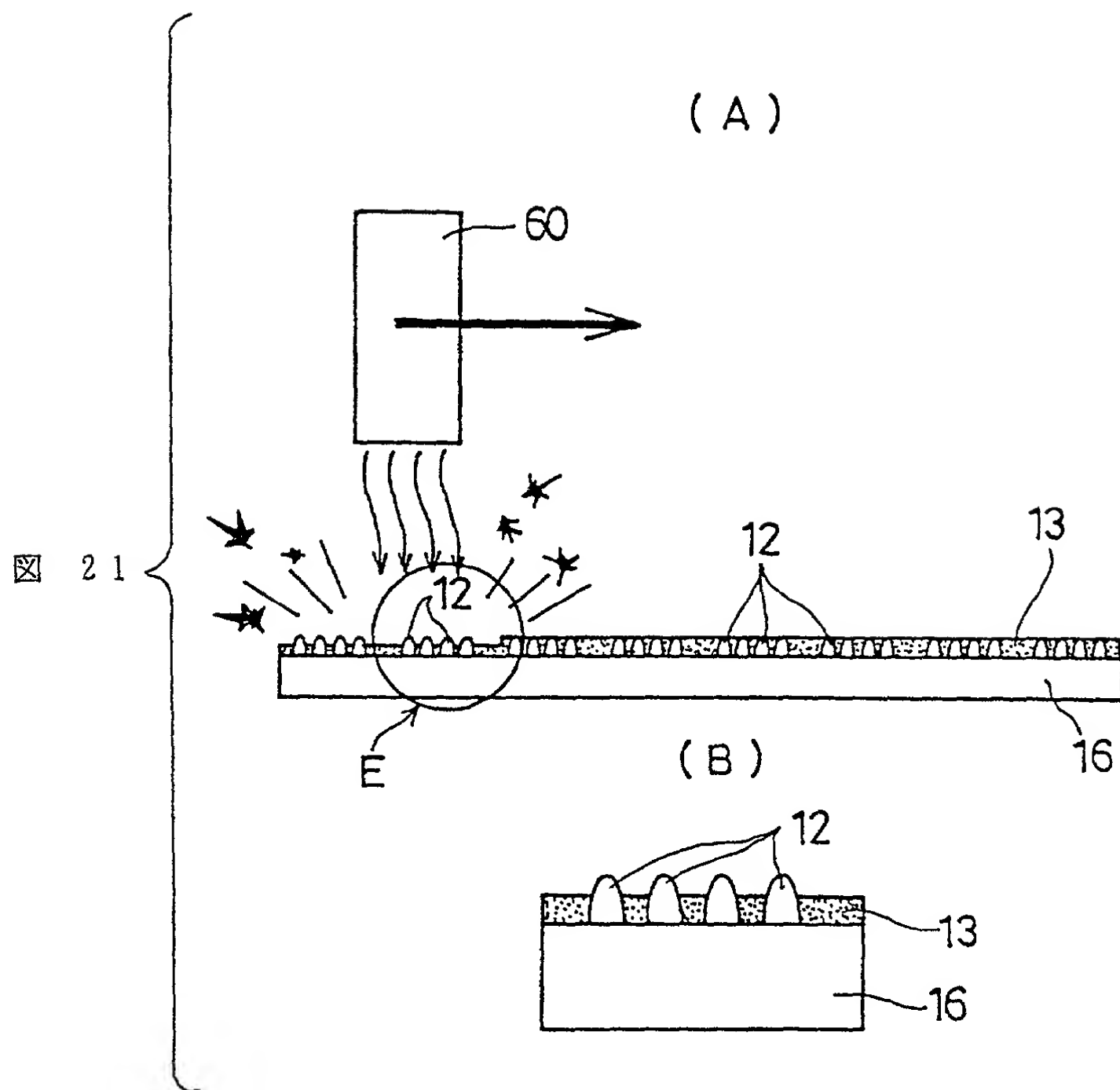


Figure 15

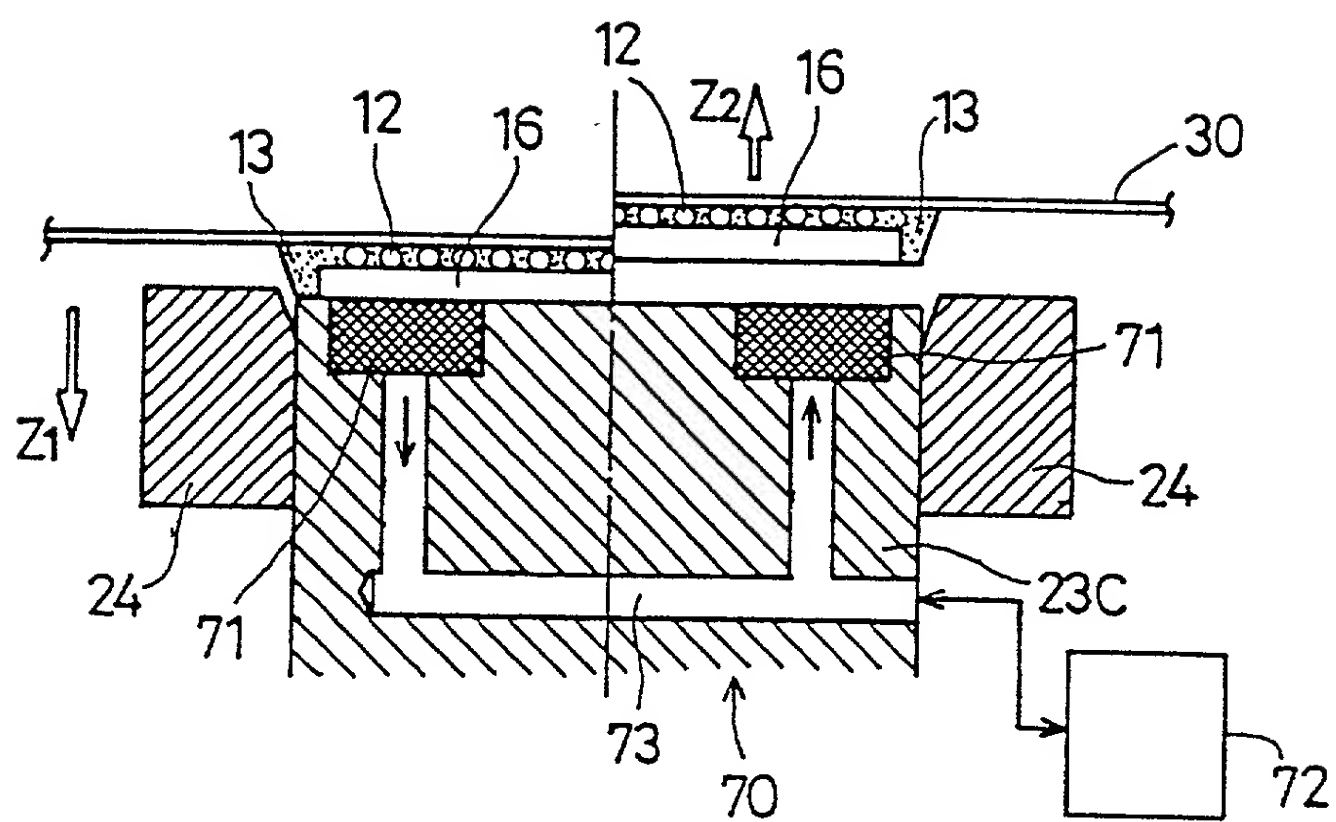




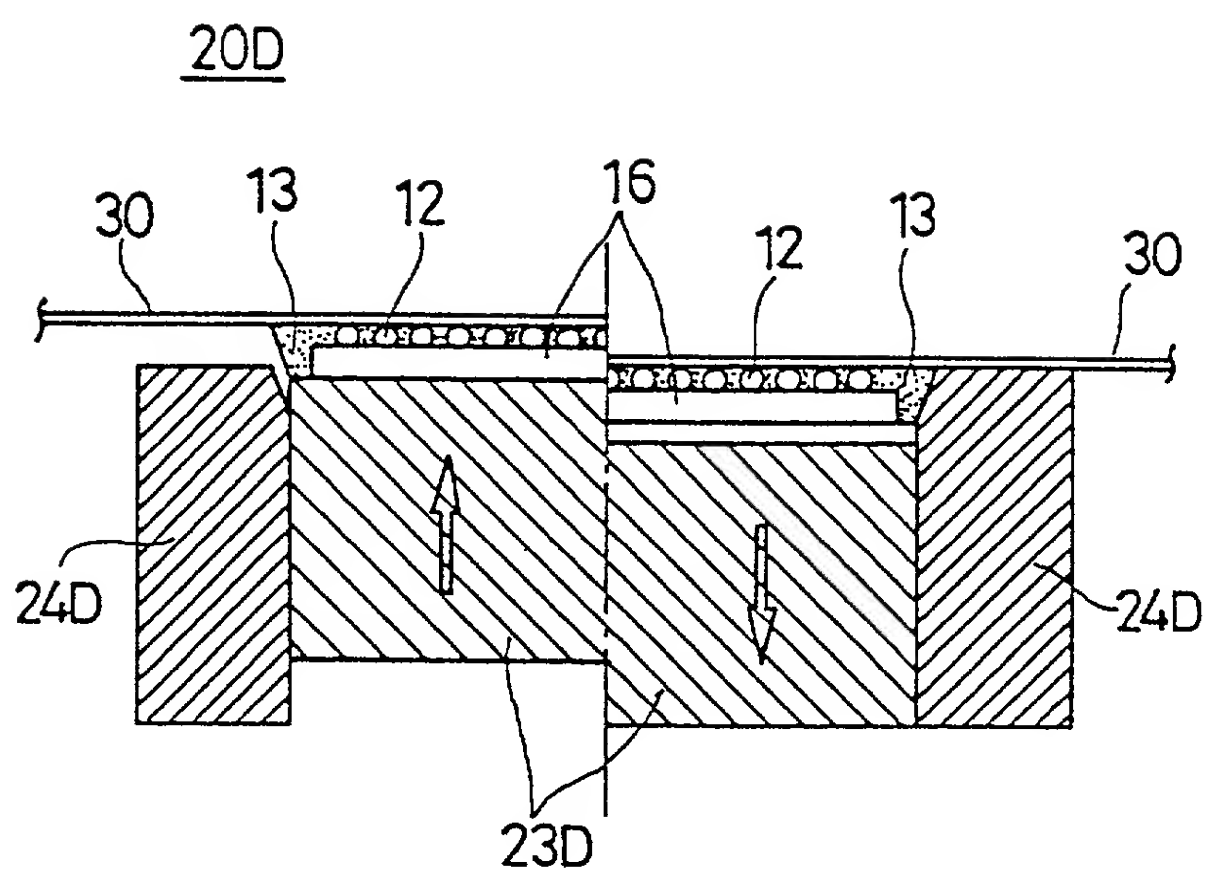


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20C



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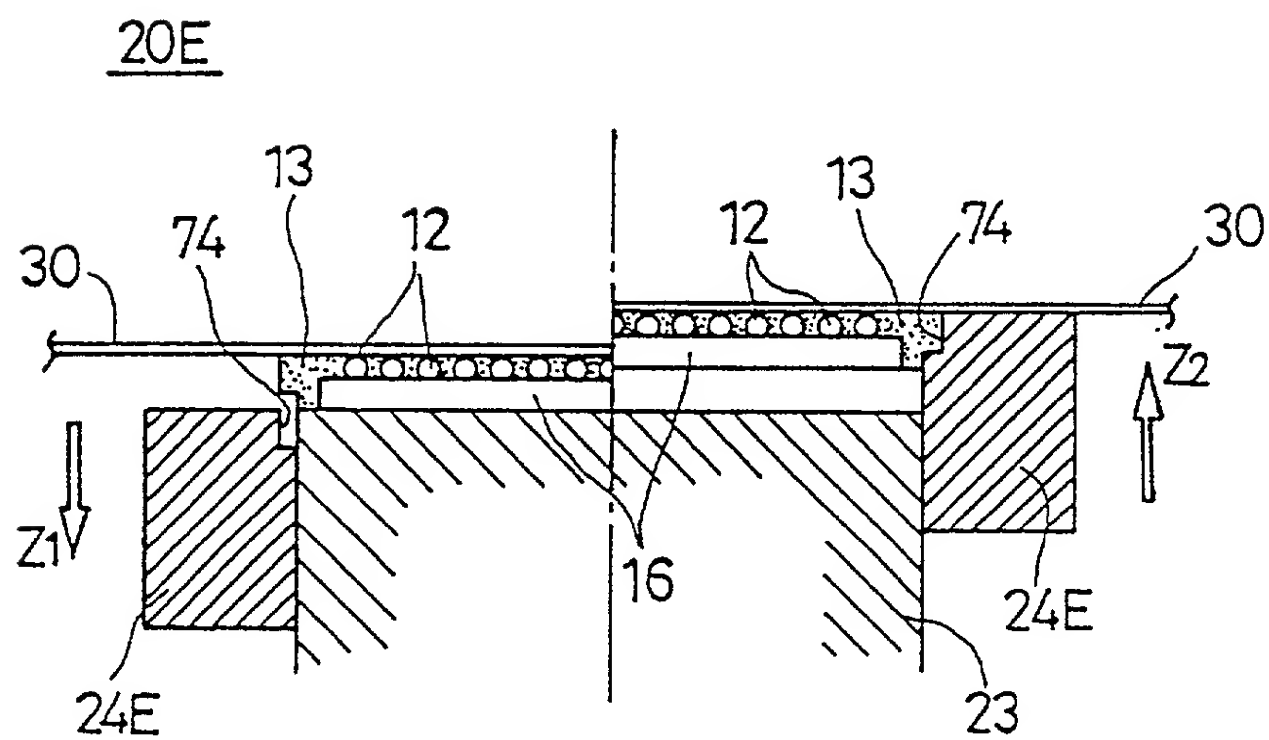


図 25

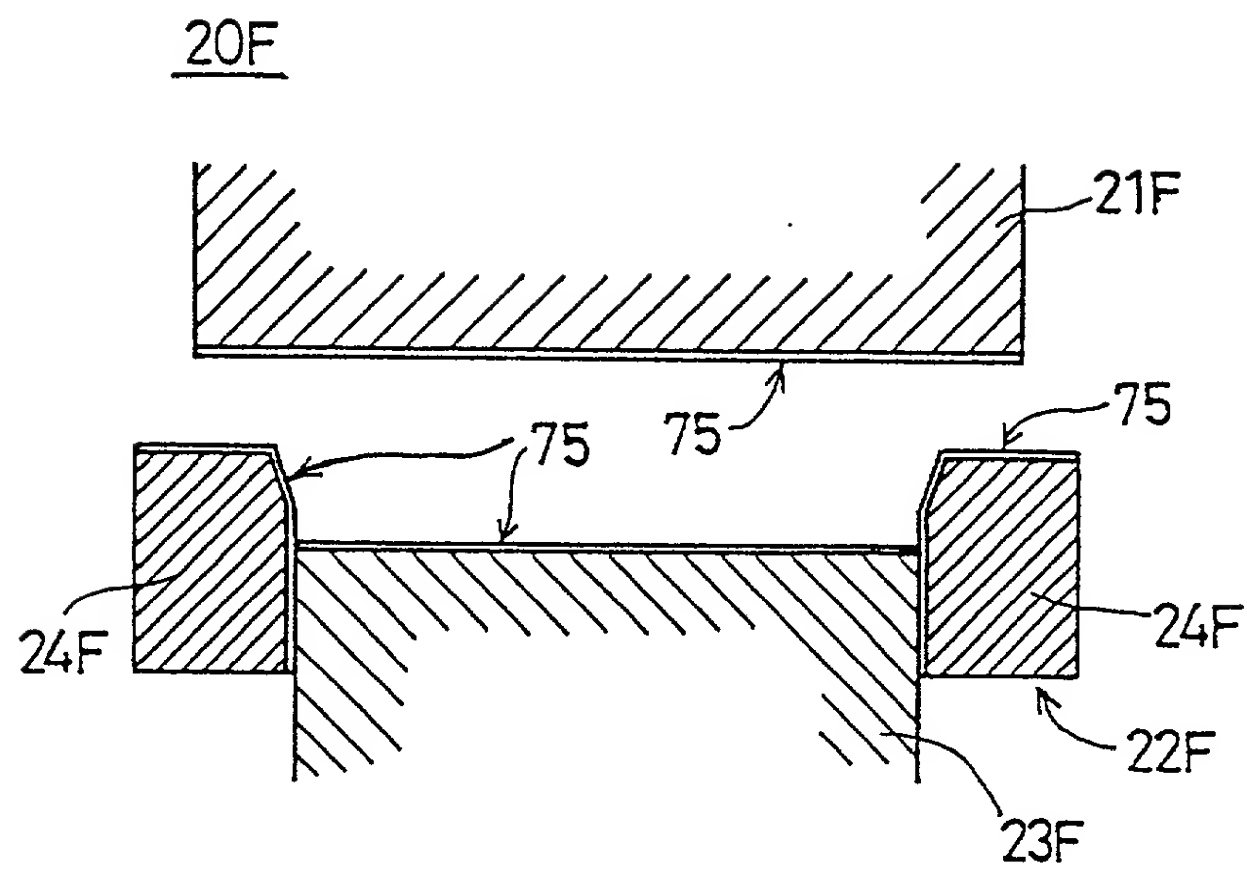
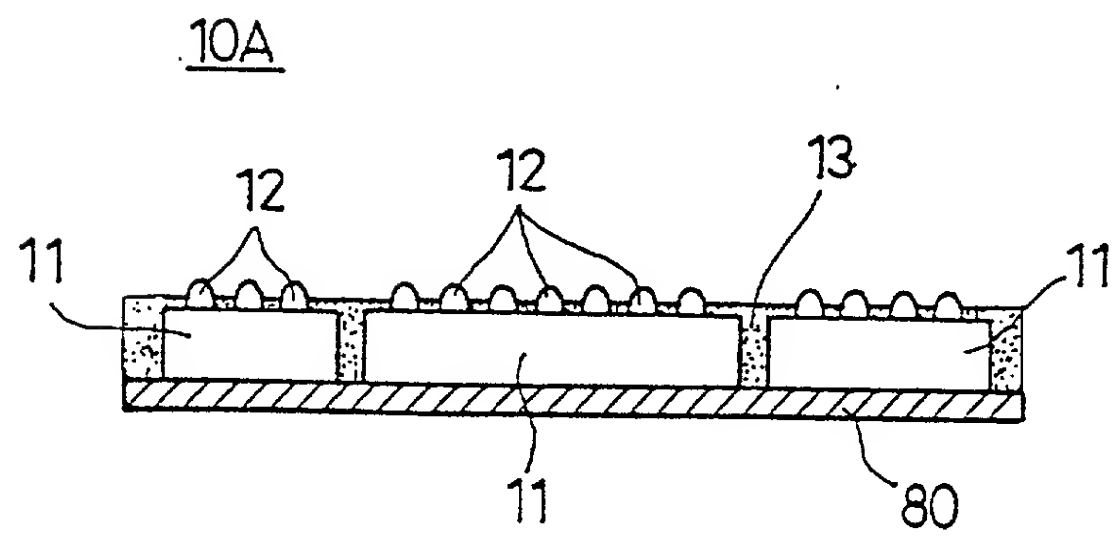
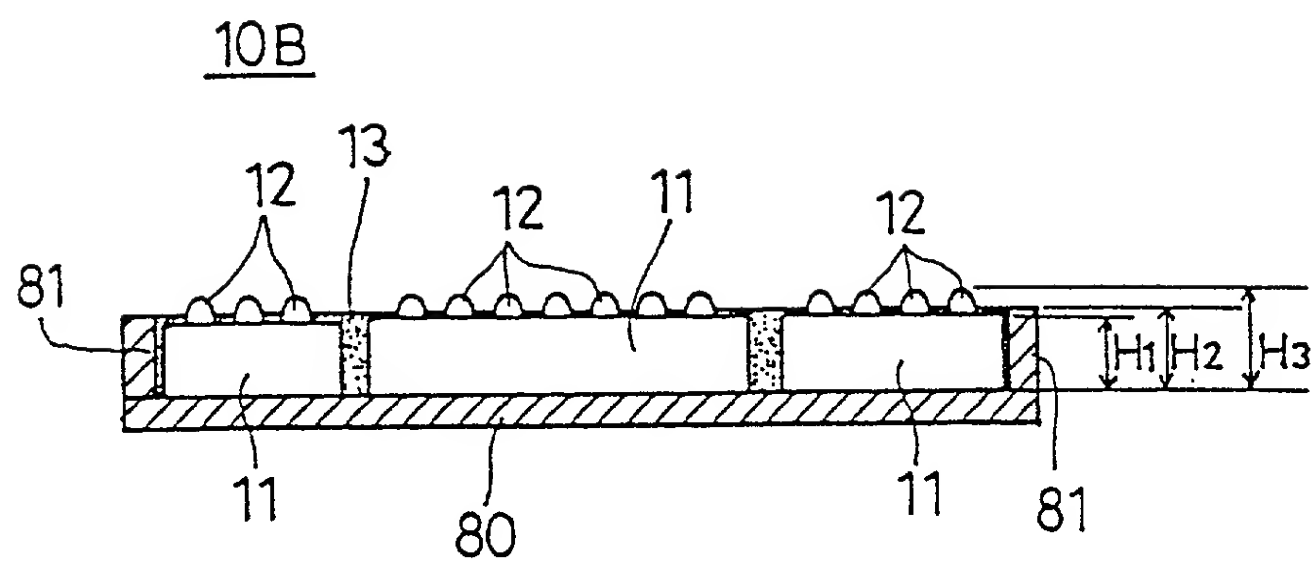


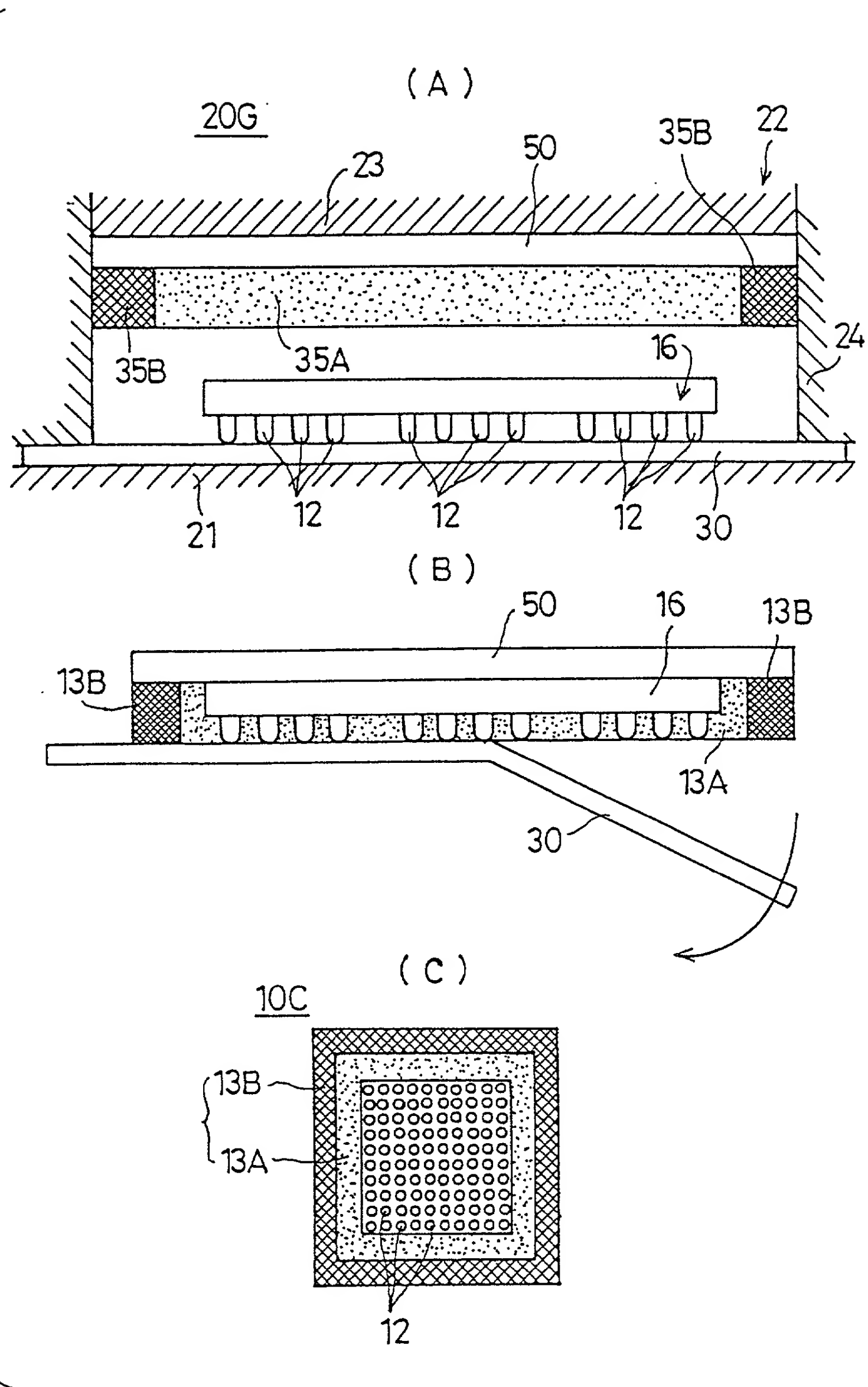
図 26



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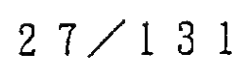


Figure 33 is a cross-sectional view of a semiconductor device in a third stage of manufacturing.

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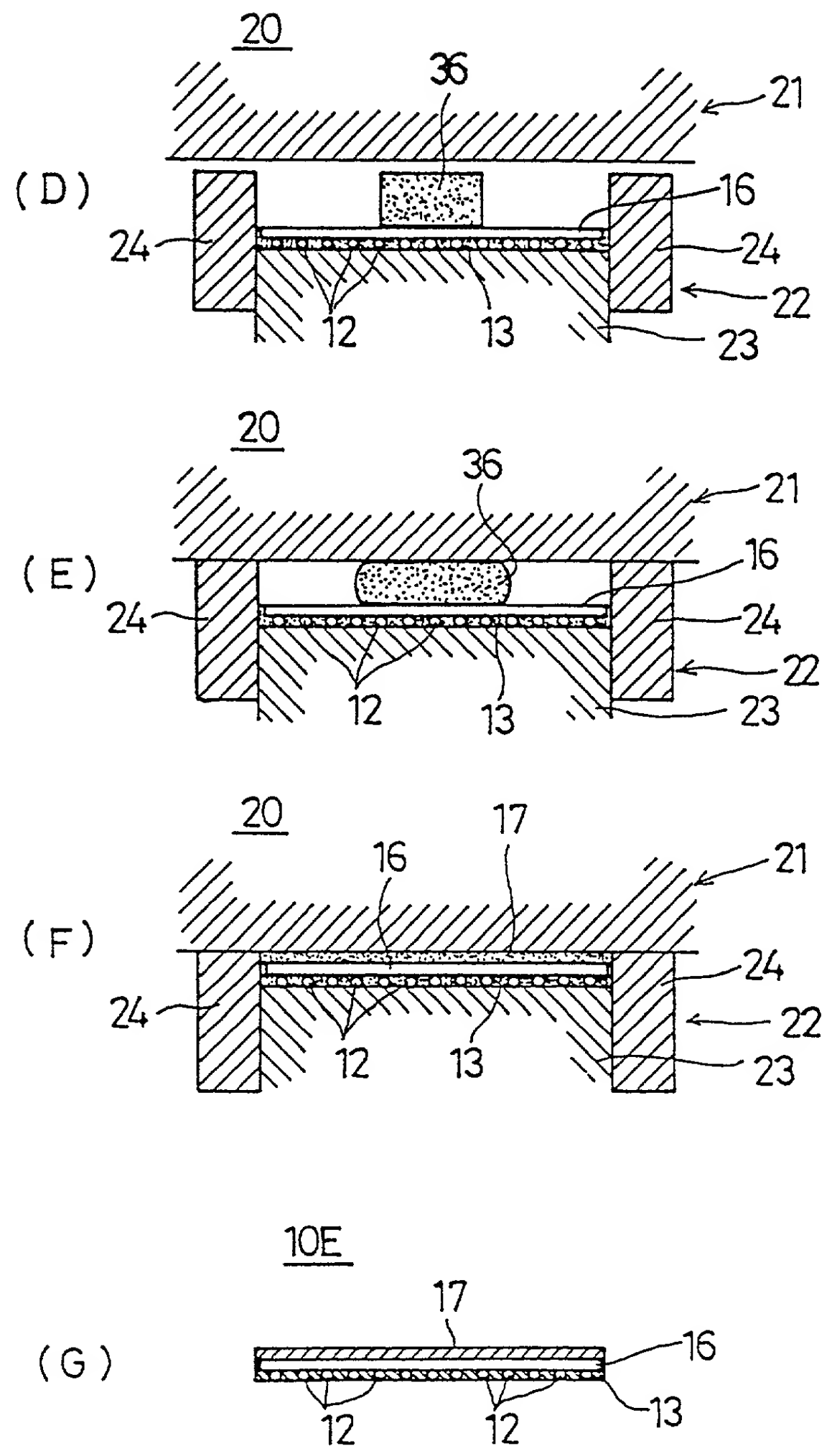


Fig. 38 is a cross-sectional view of a semiconductor device in a first stage of a manufacturing process.

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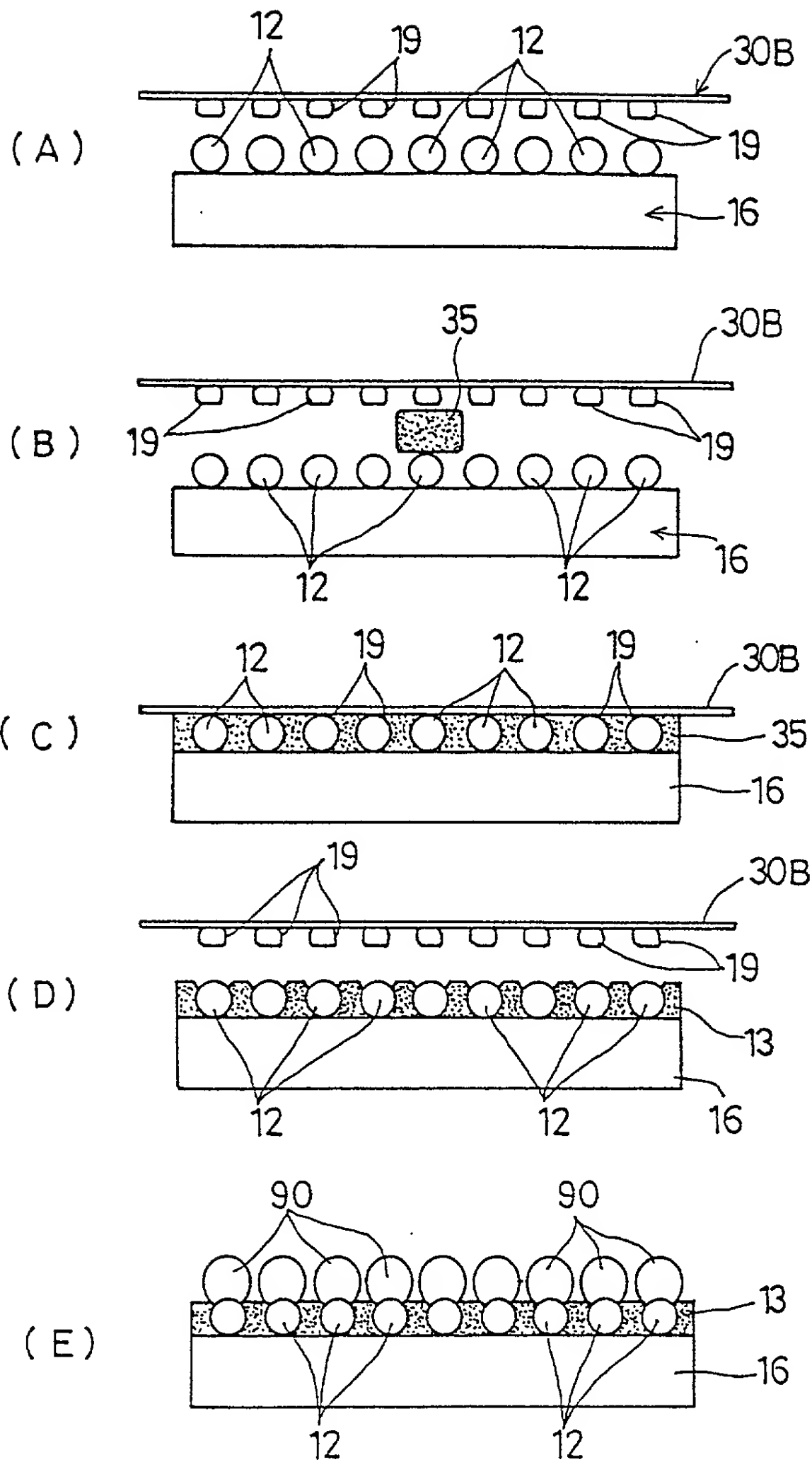


图 40

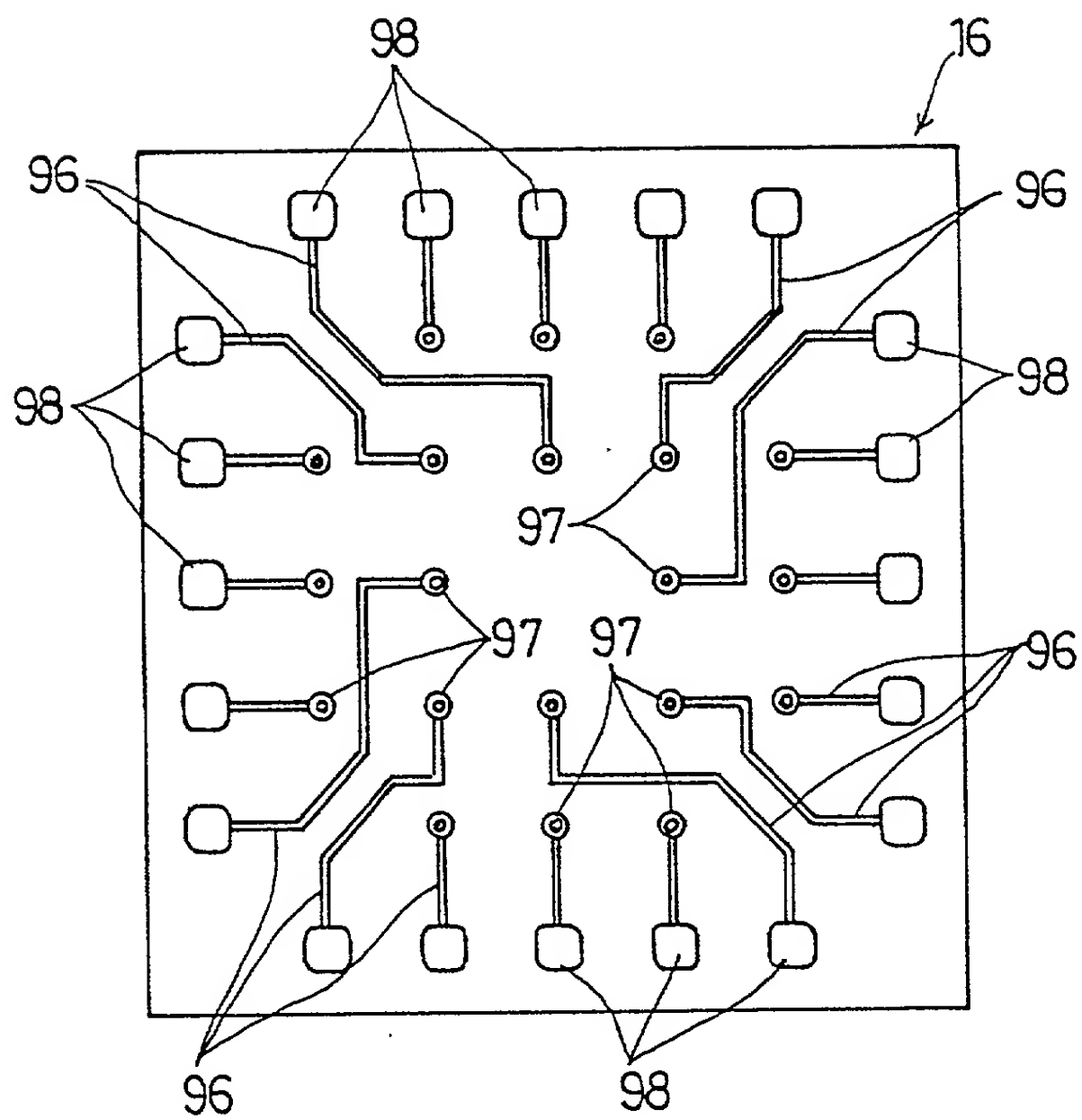
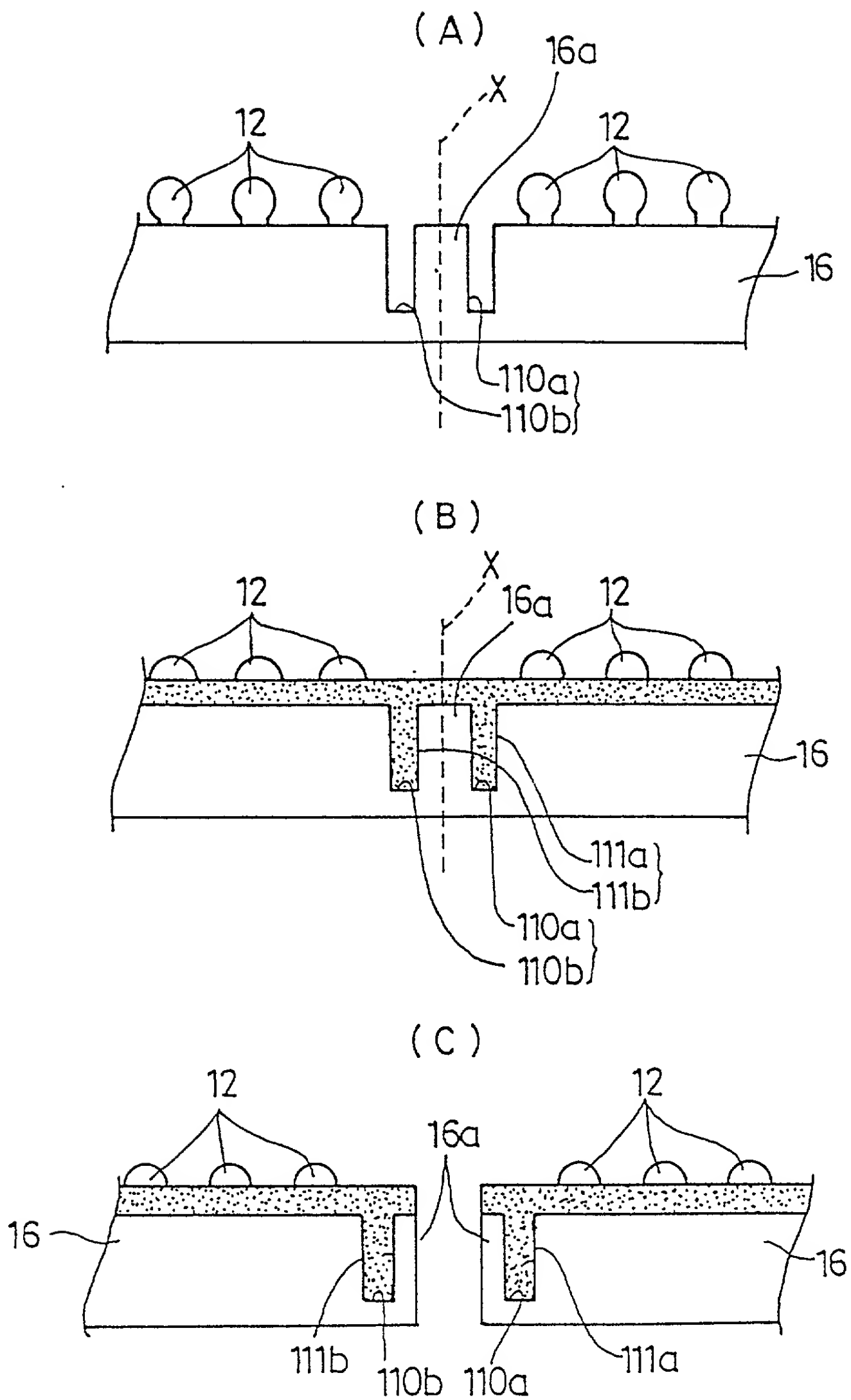


図 42



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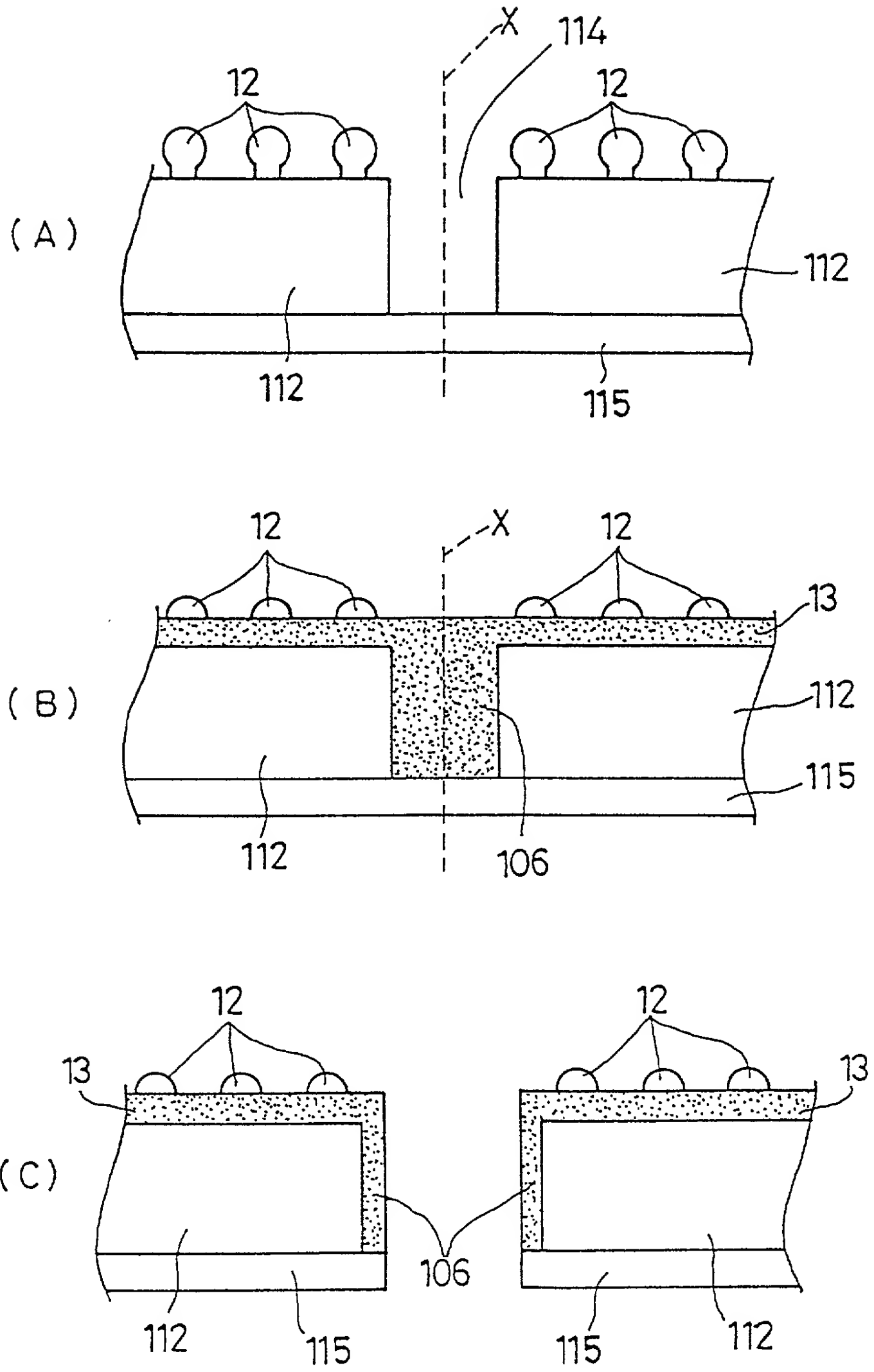
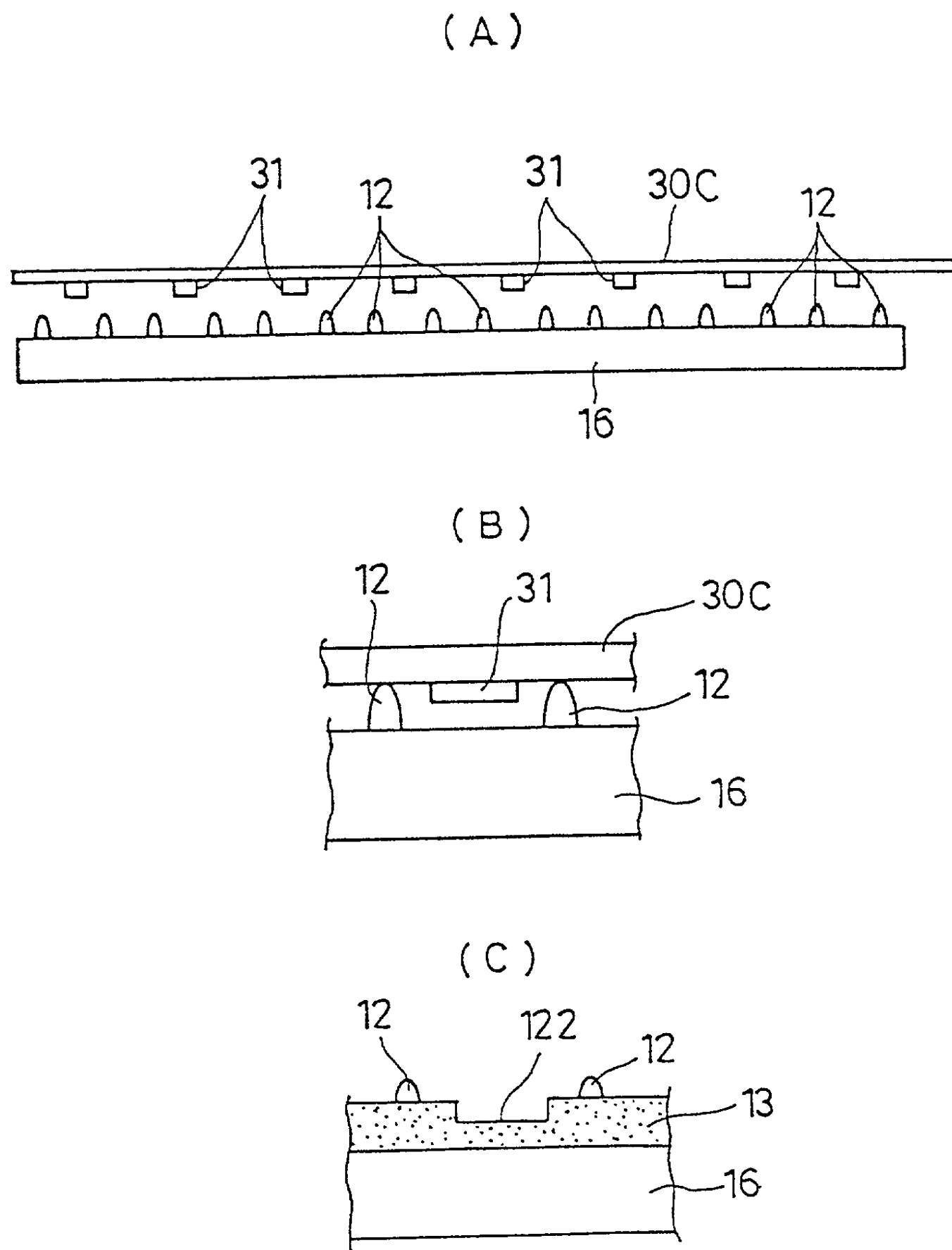


Figure 48 is a schematic diagram of a semiconductor device in three cross-sectional views (A), (B), and (C).

図 48



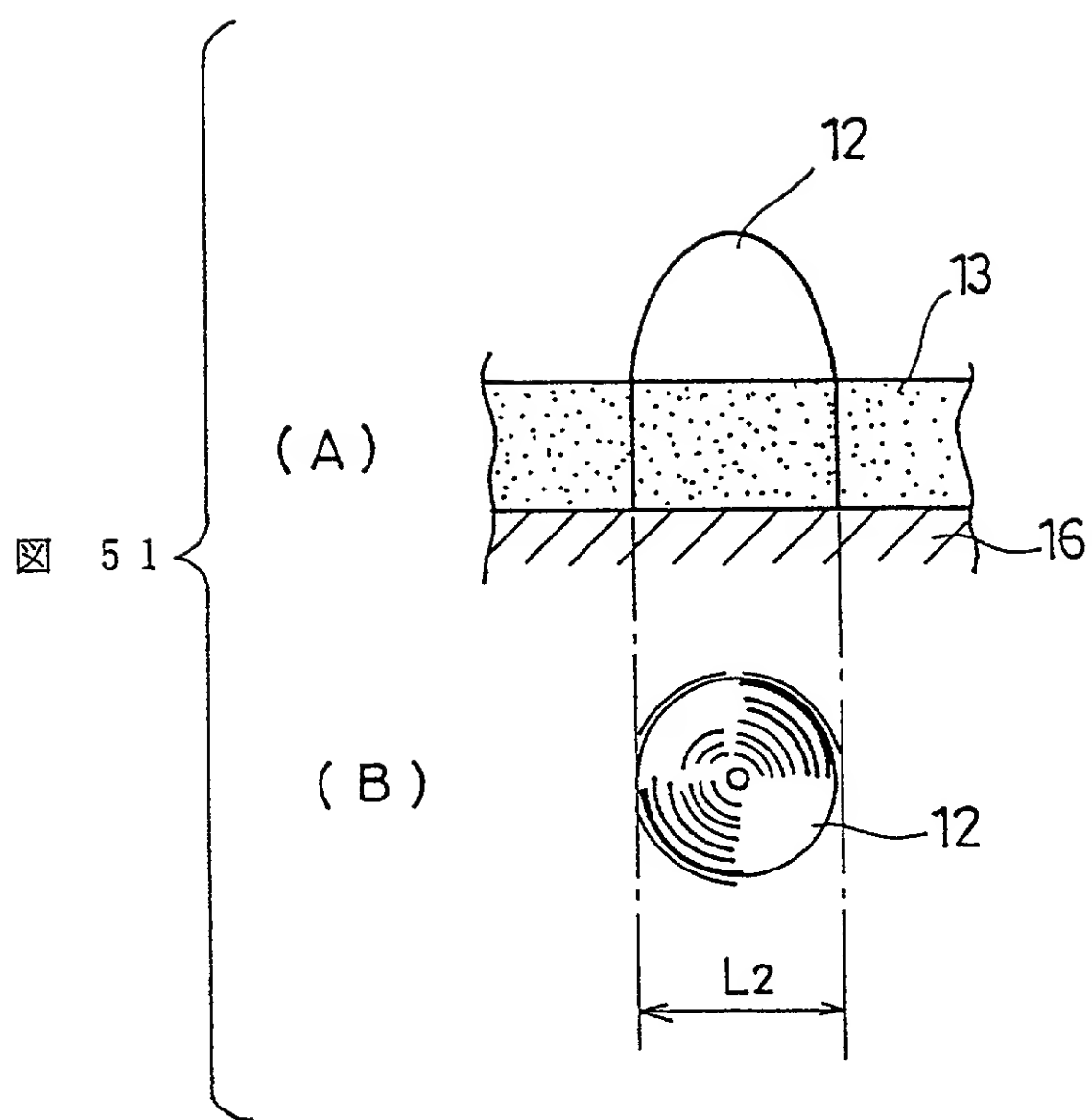
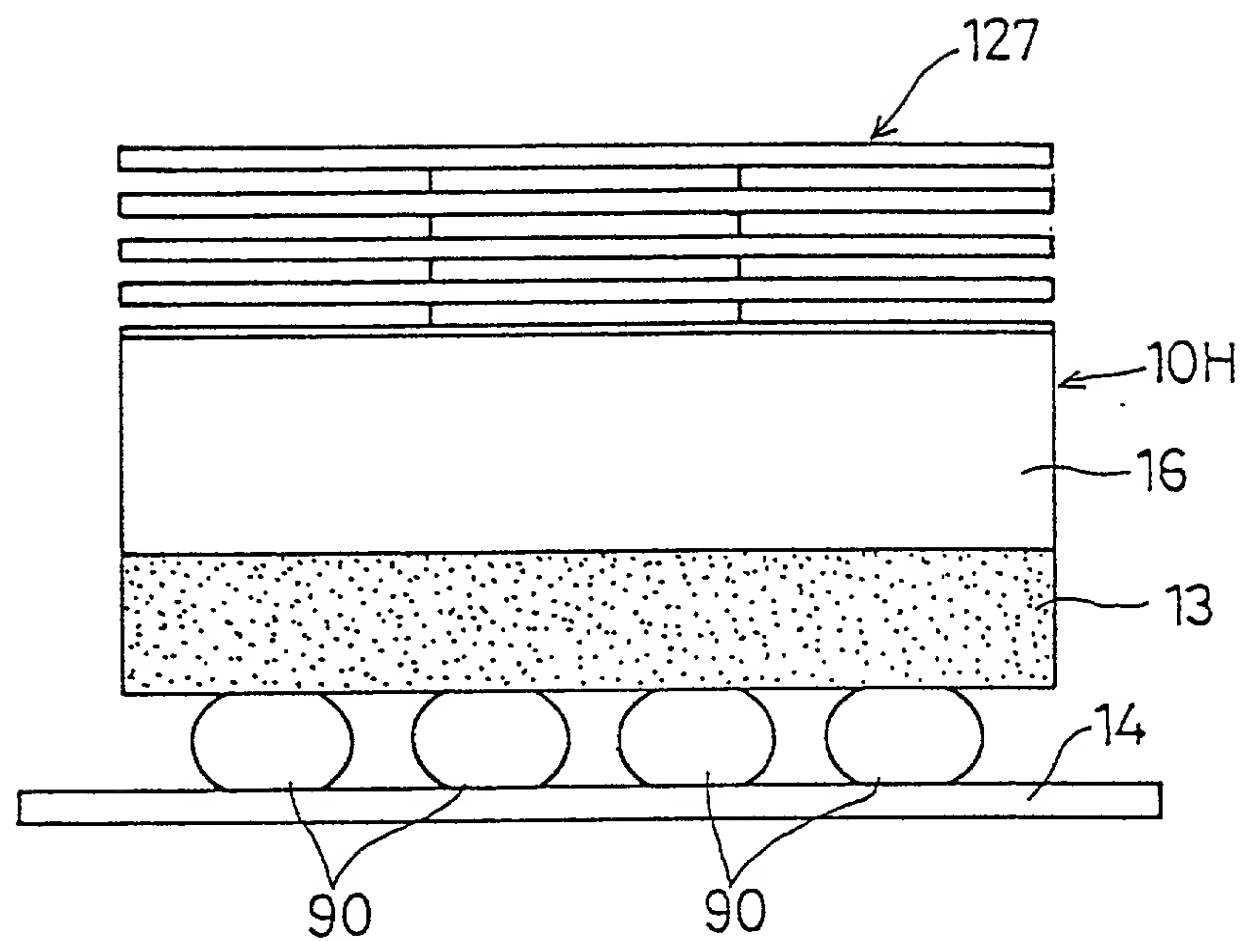


Fig. 48 is a cross-sectional view of a display device according to the present invention.

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(A)



(B)

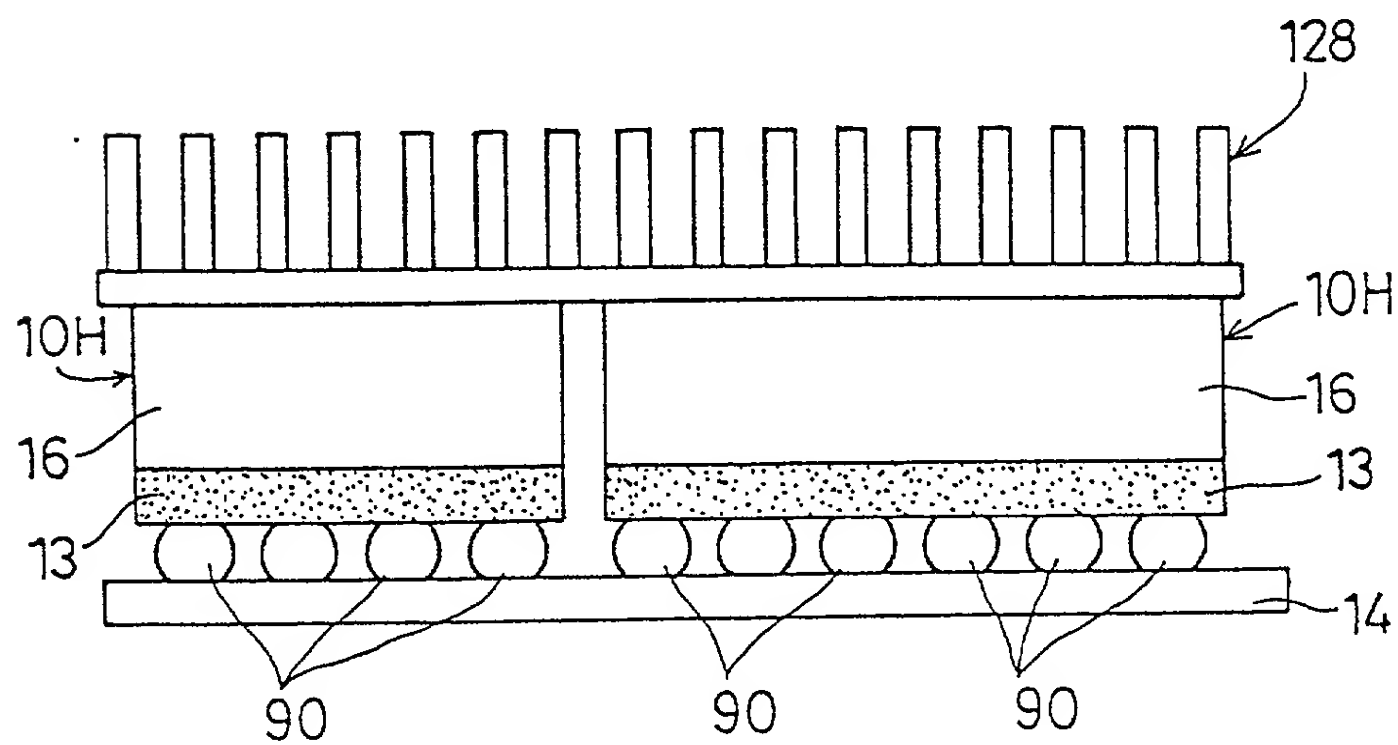


図 56

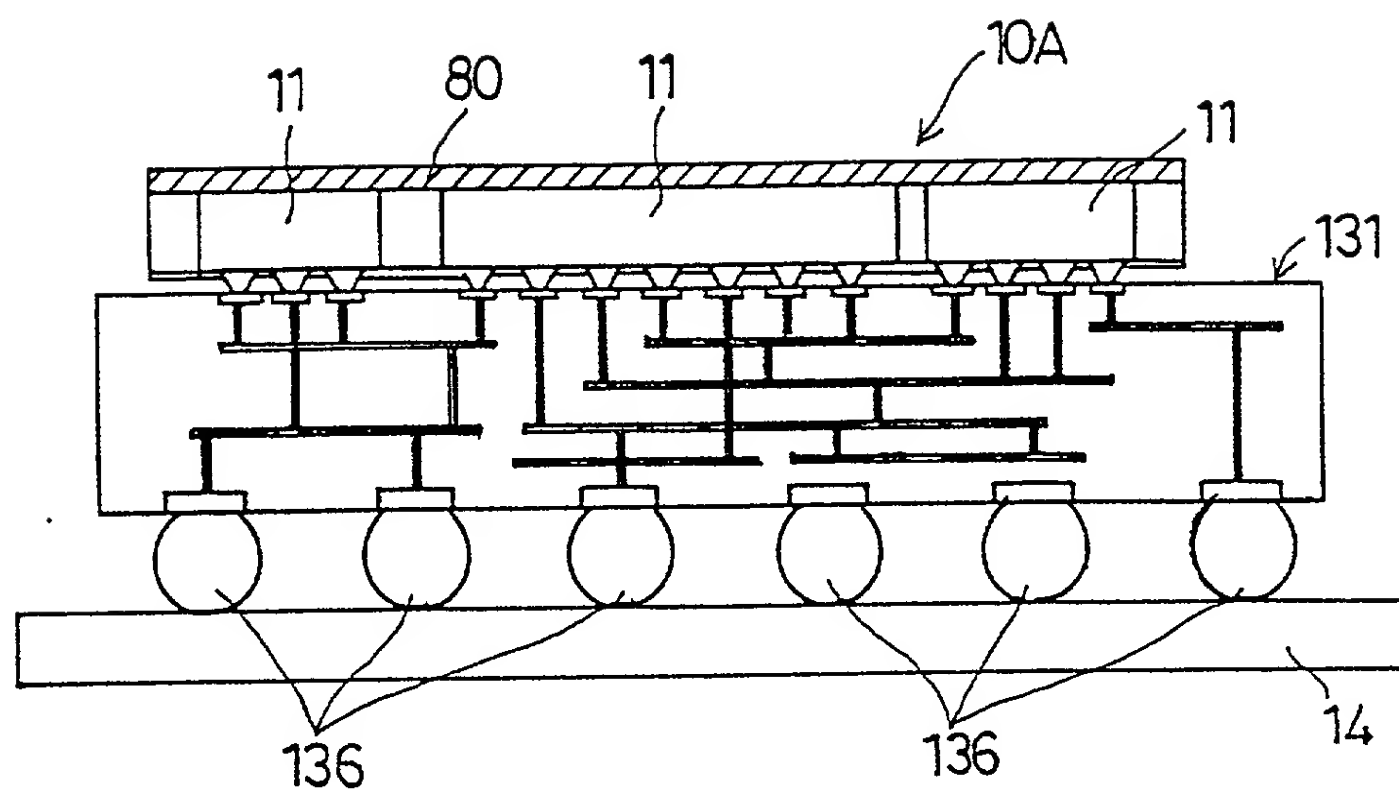
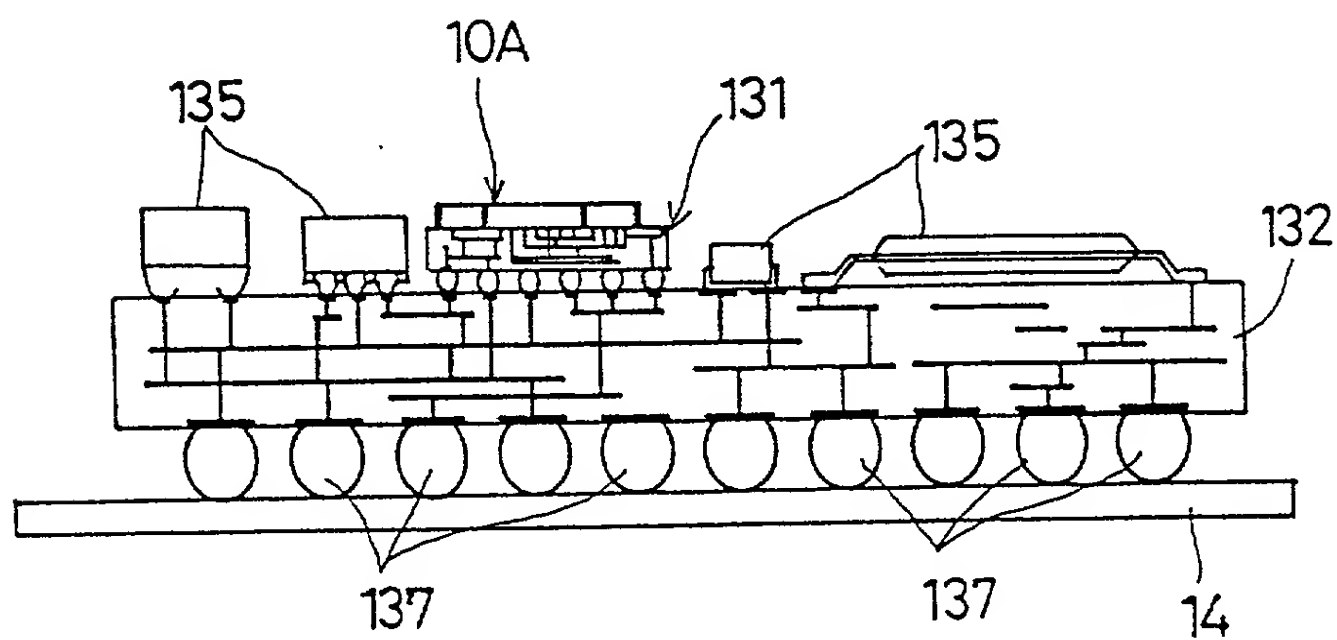
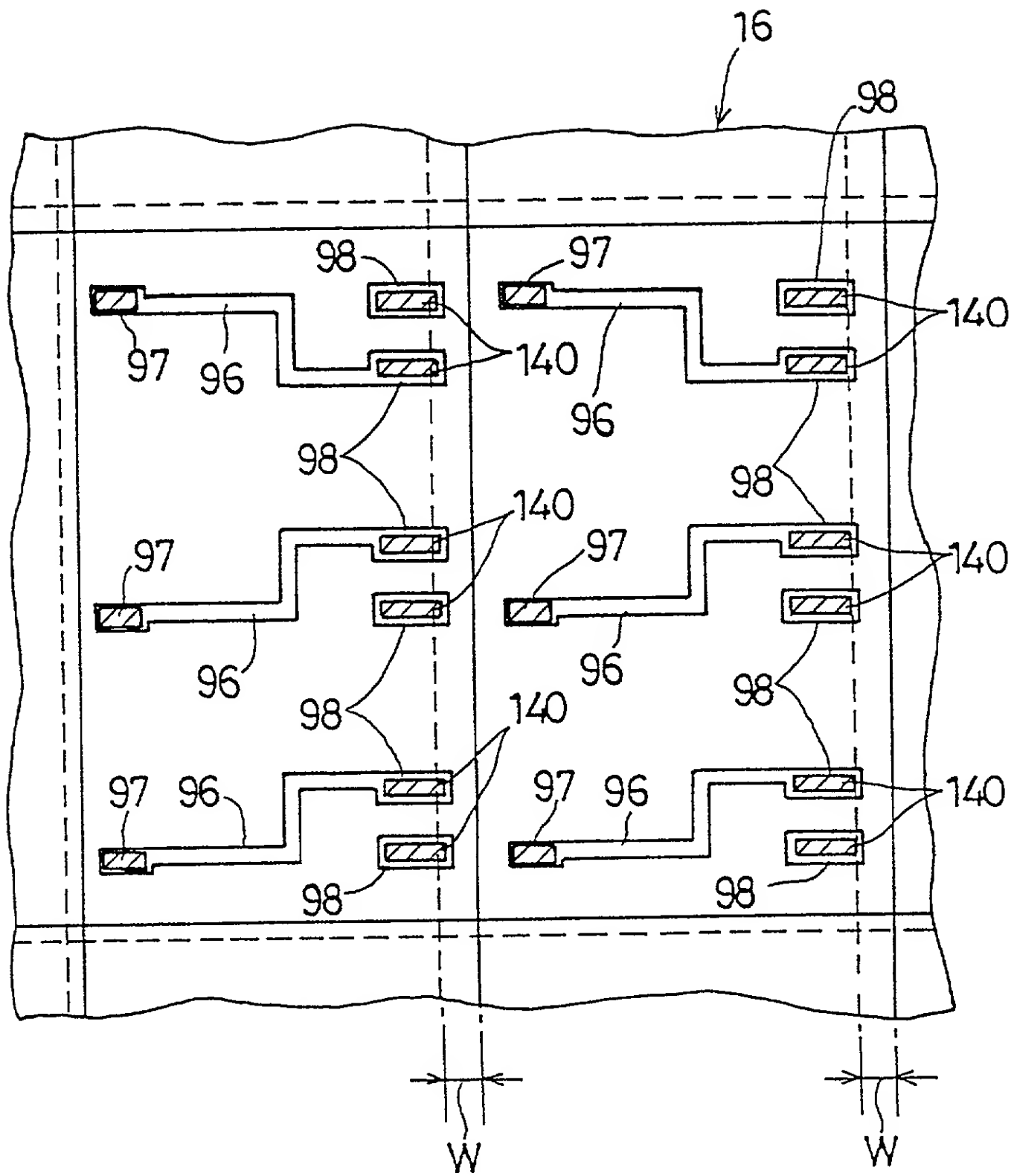
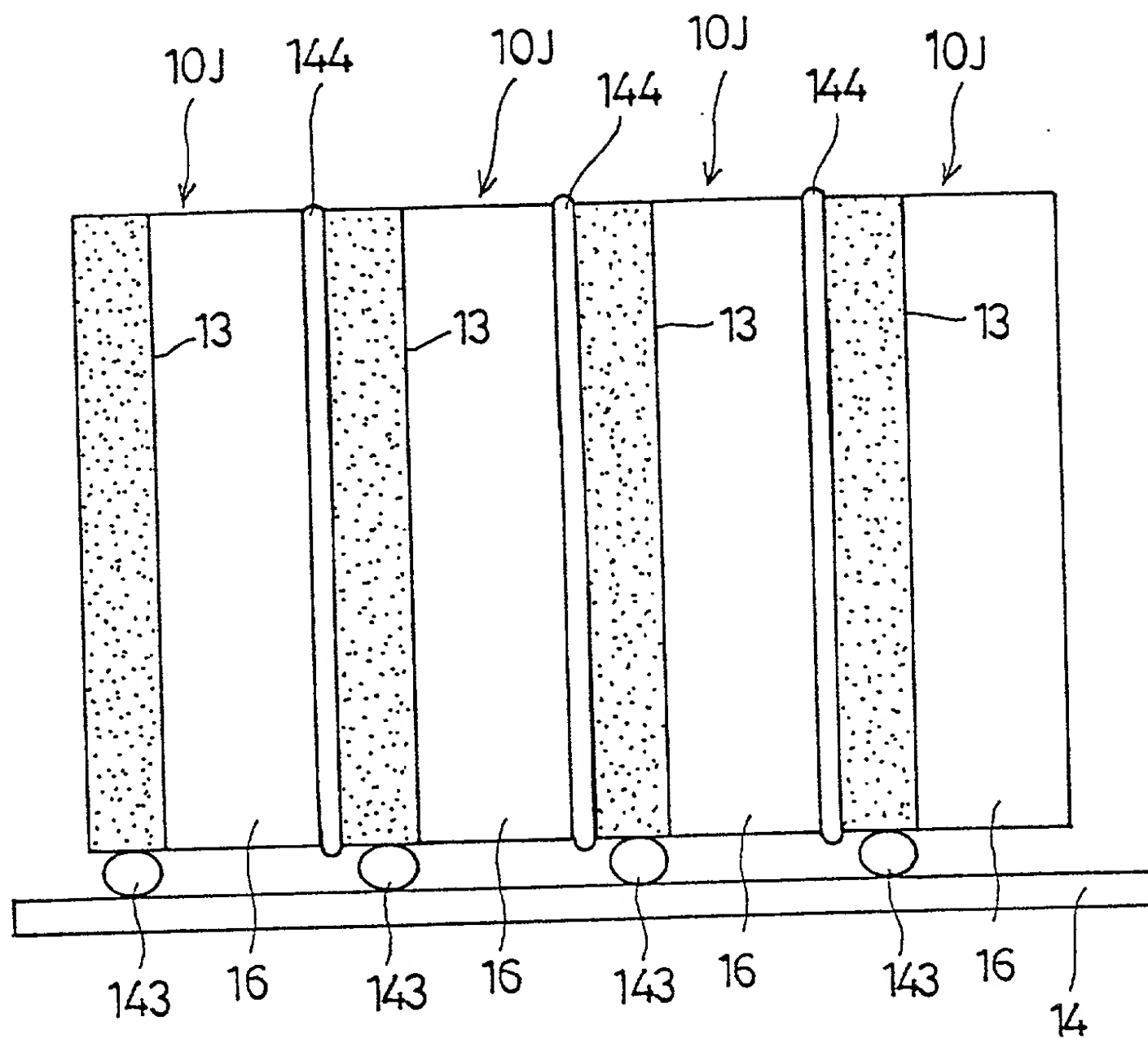


図 57

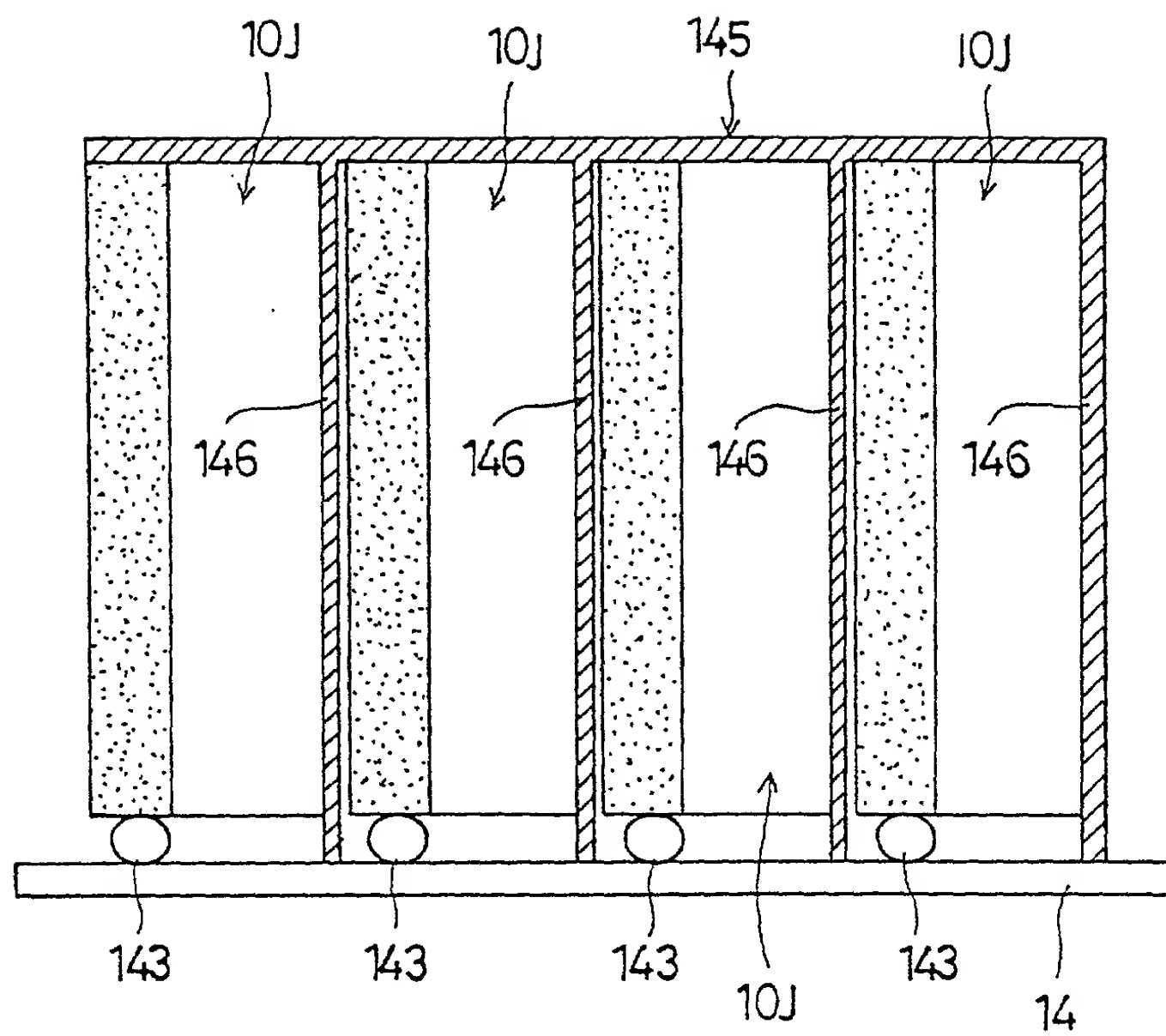




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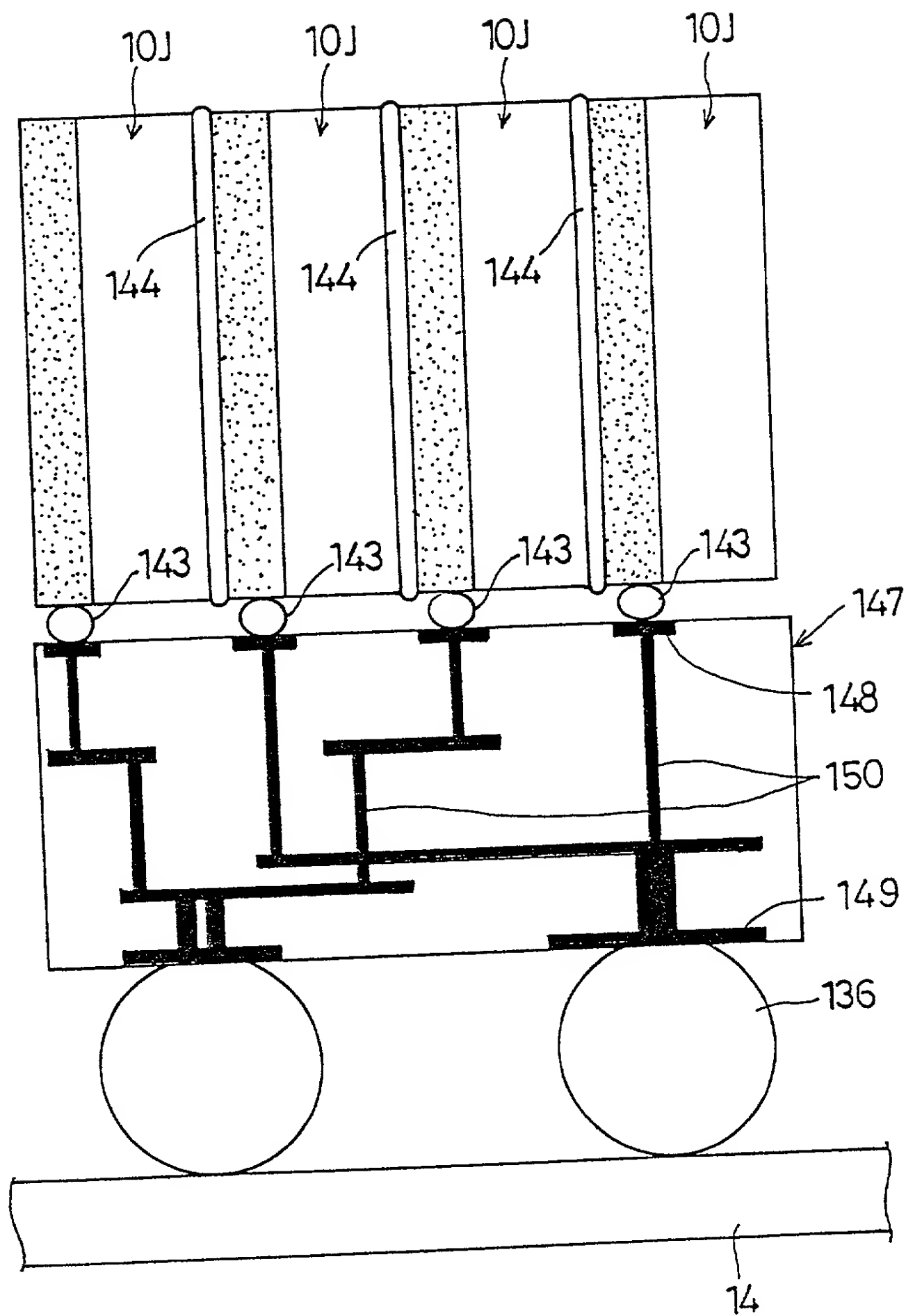


図 70

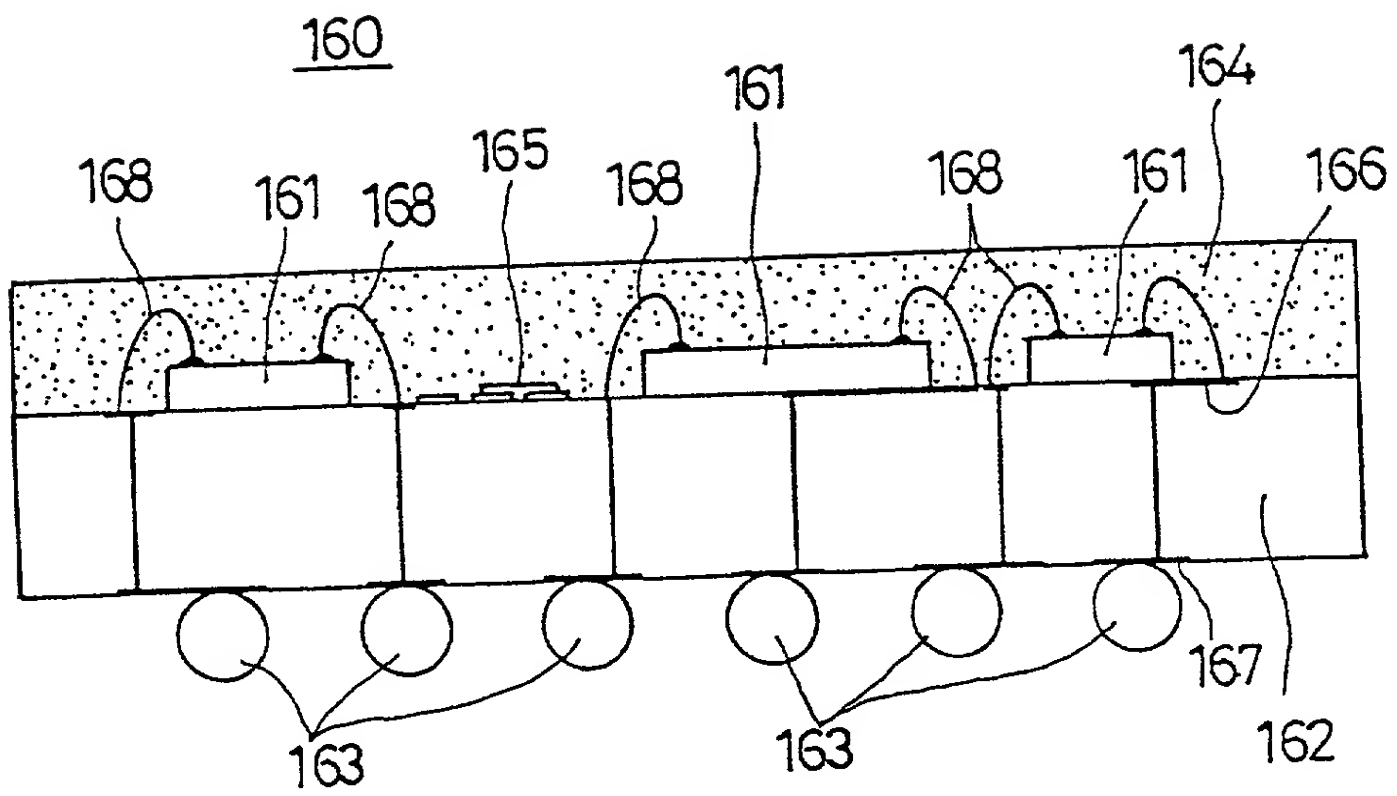
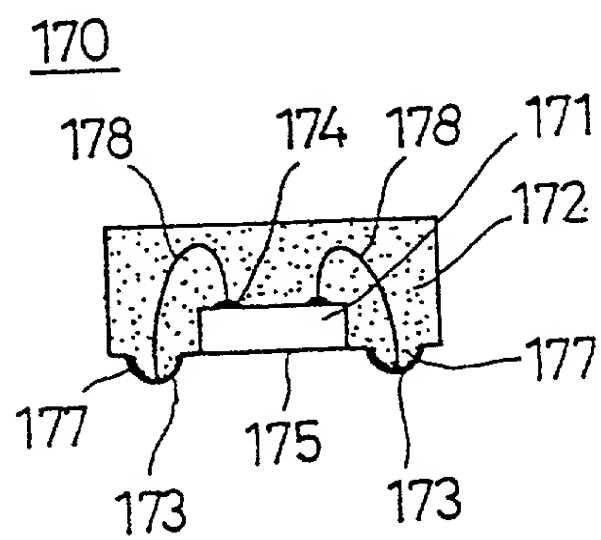


図 71



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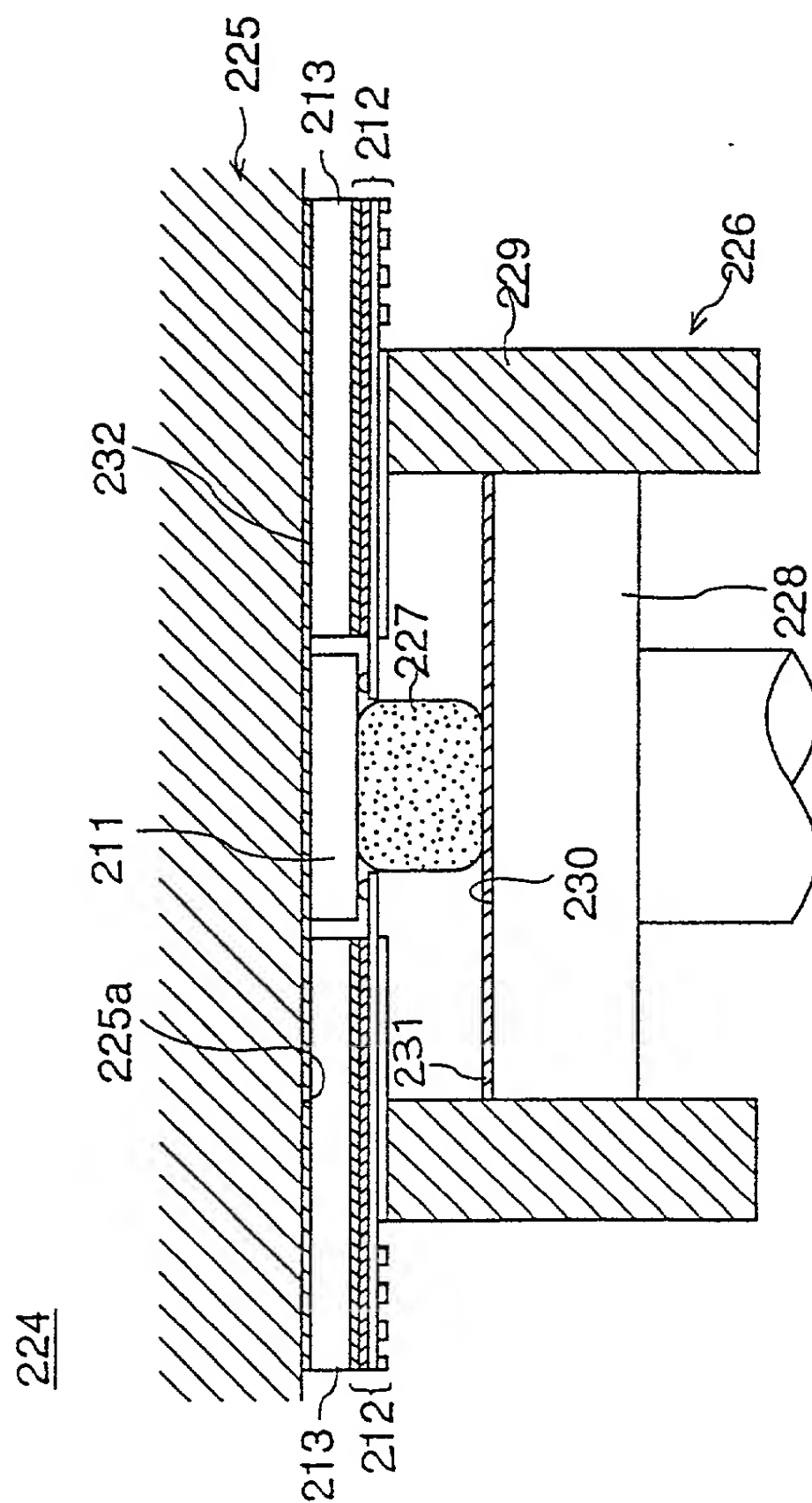


图 81

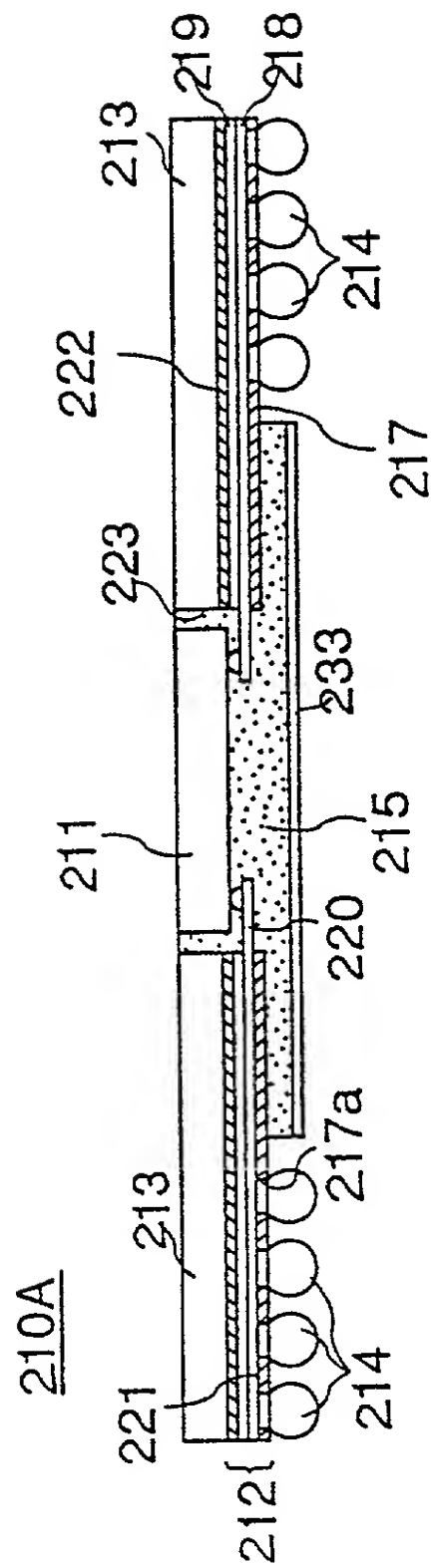
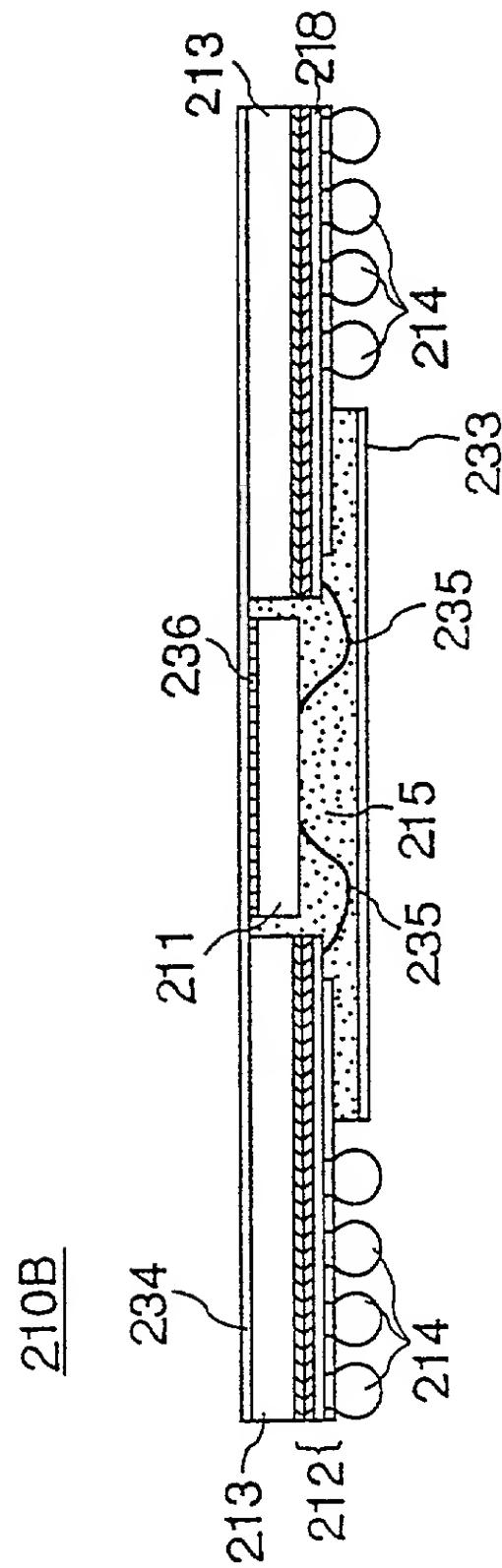


图 84



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210D

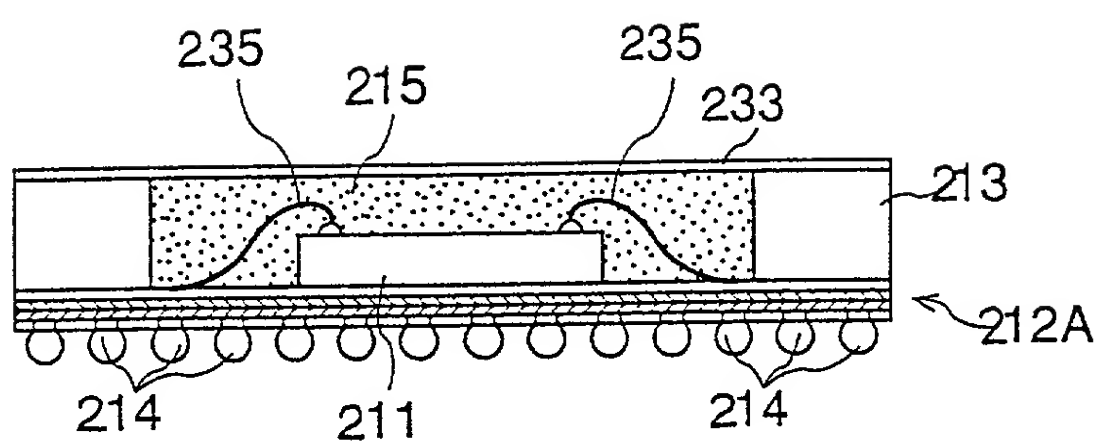
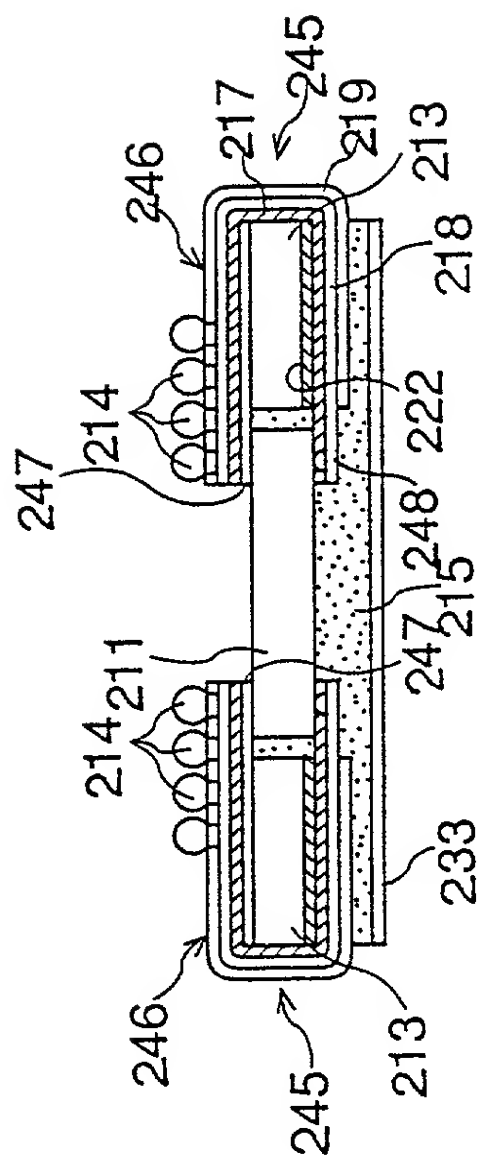


图 88

210E



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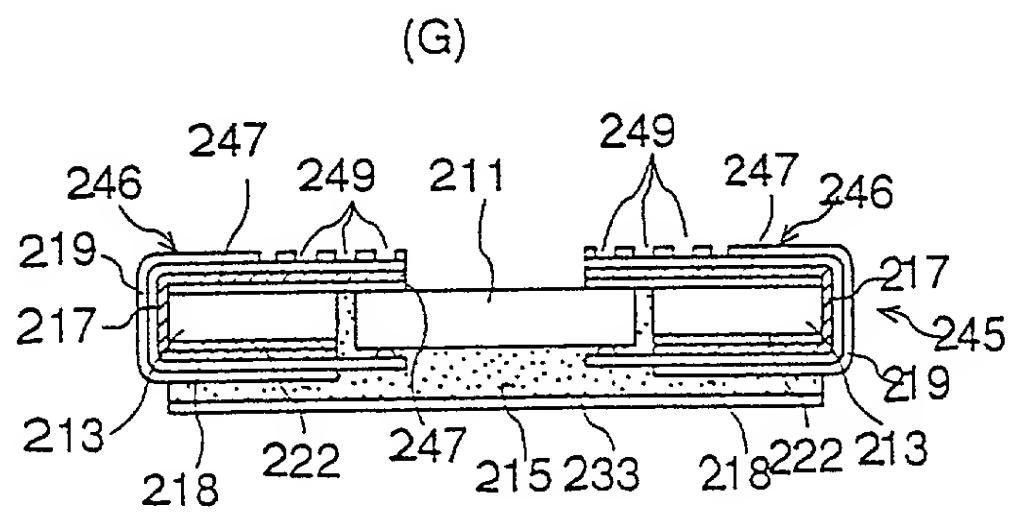
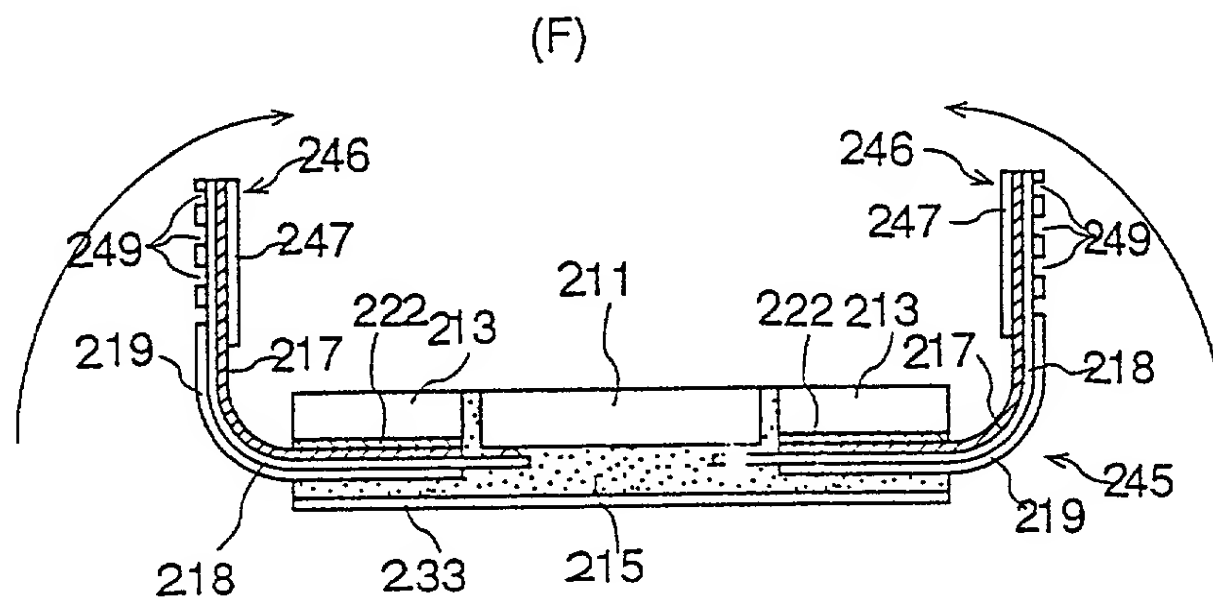
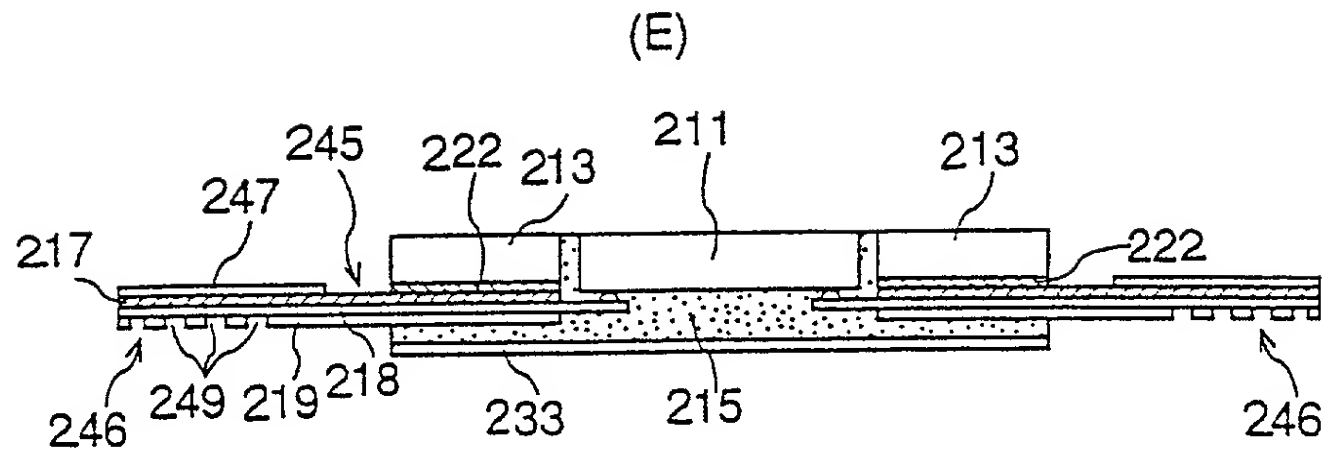
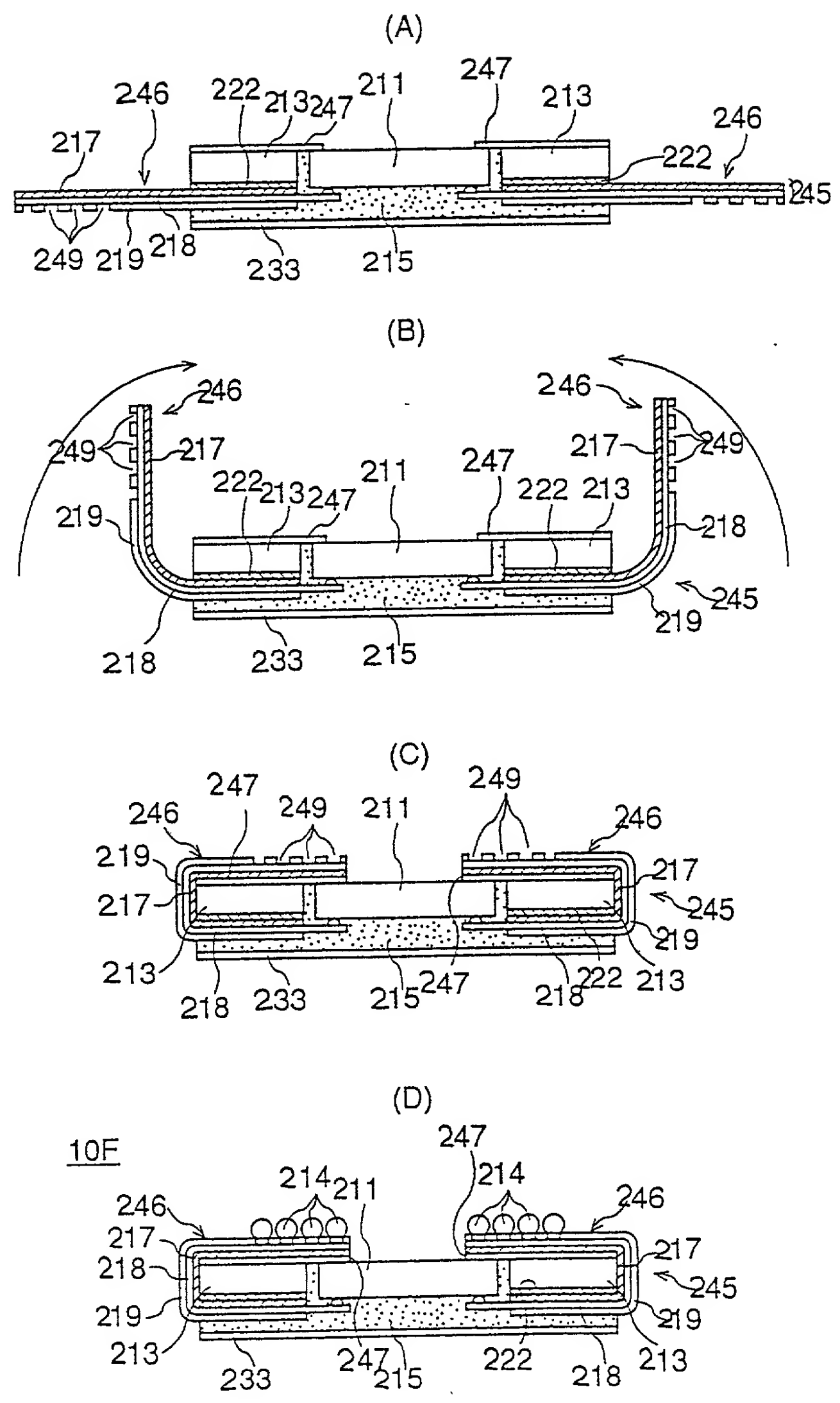


FIG. 91

FIG. 91



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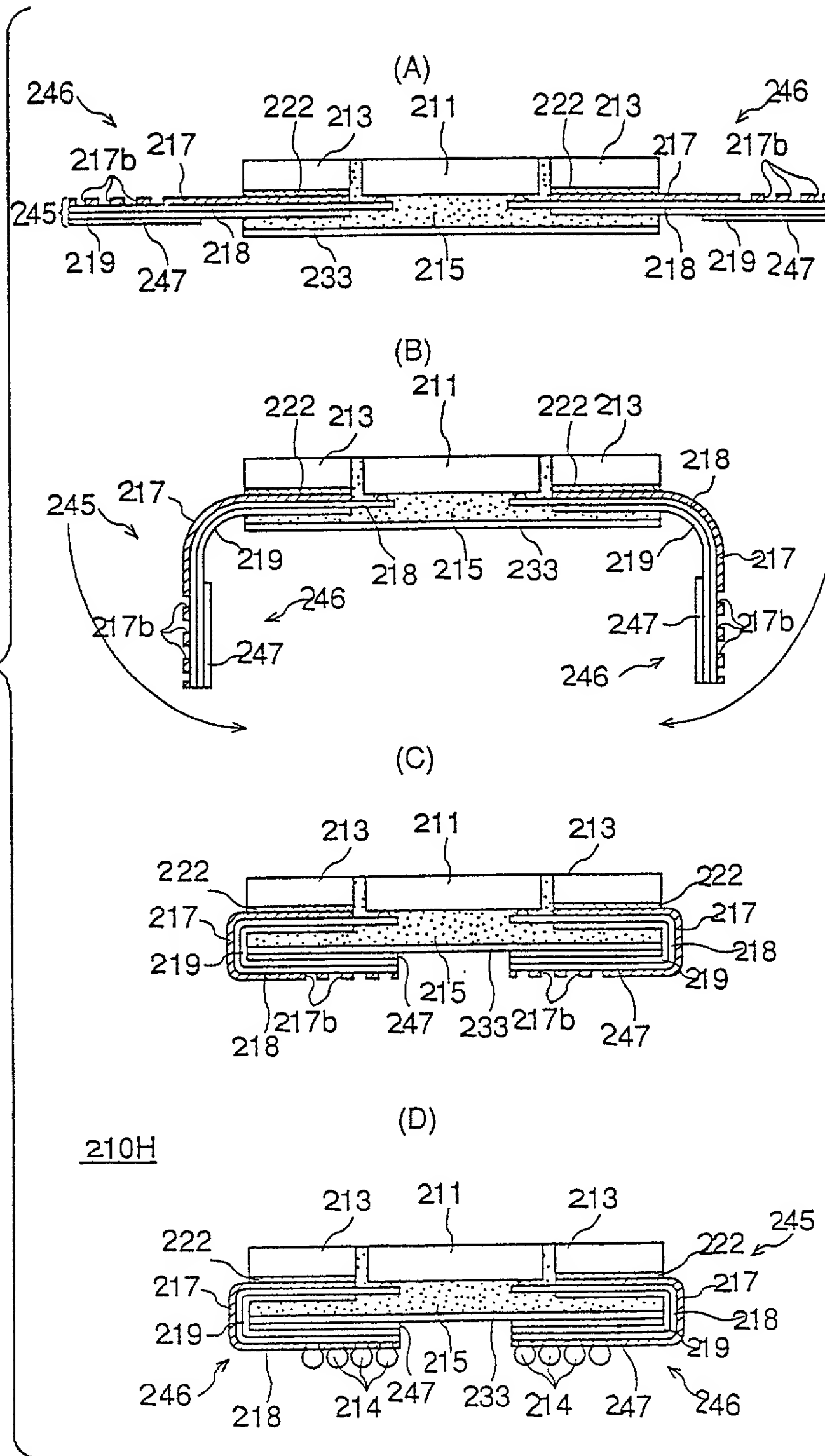
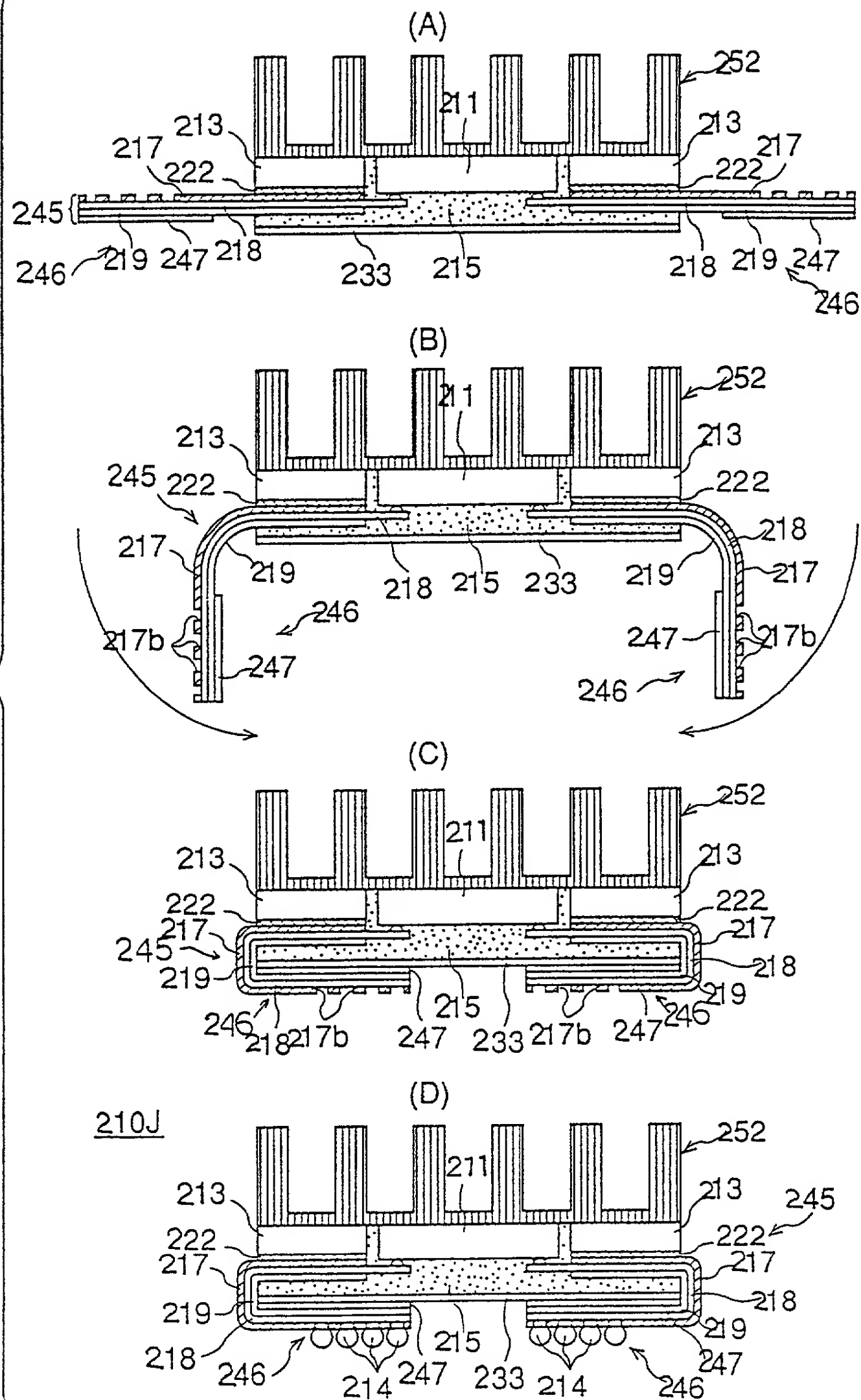
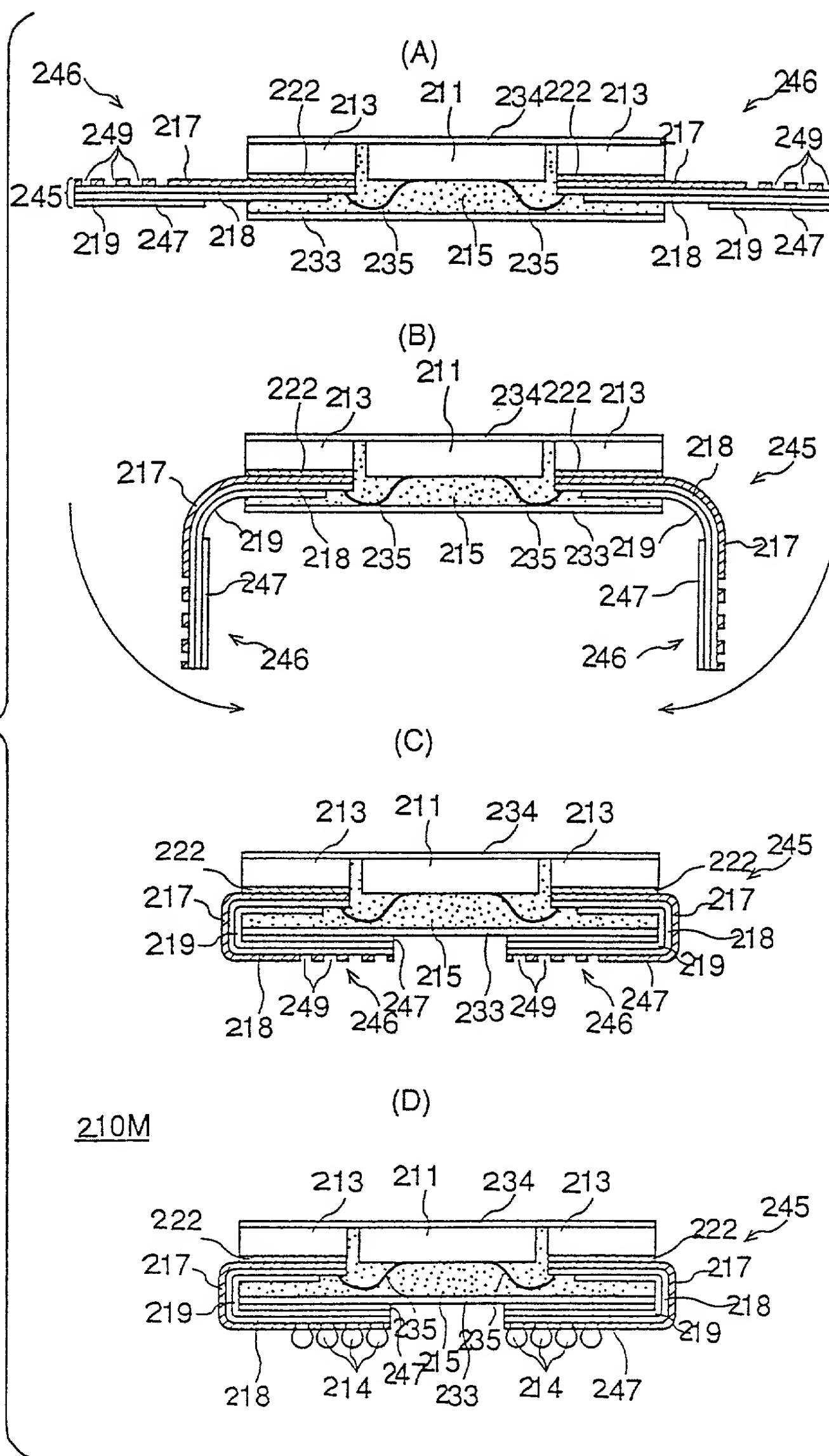
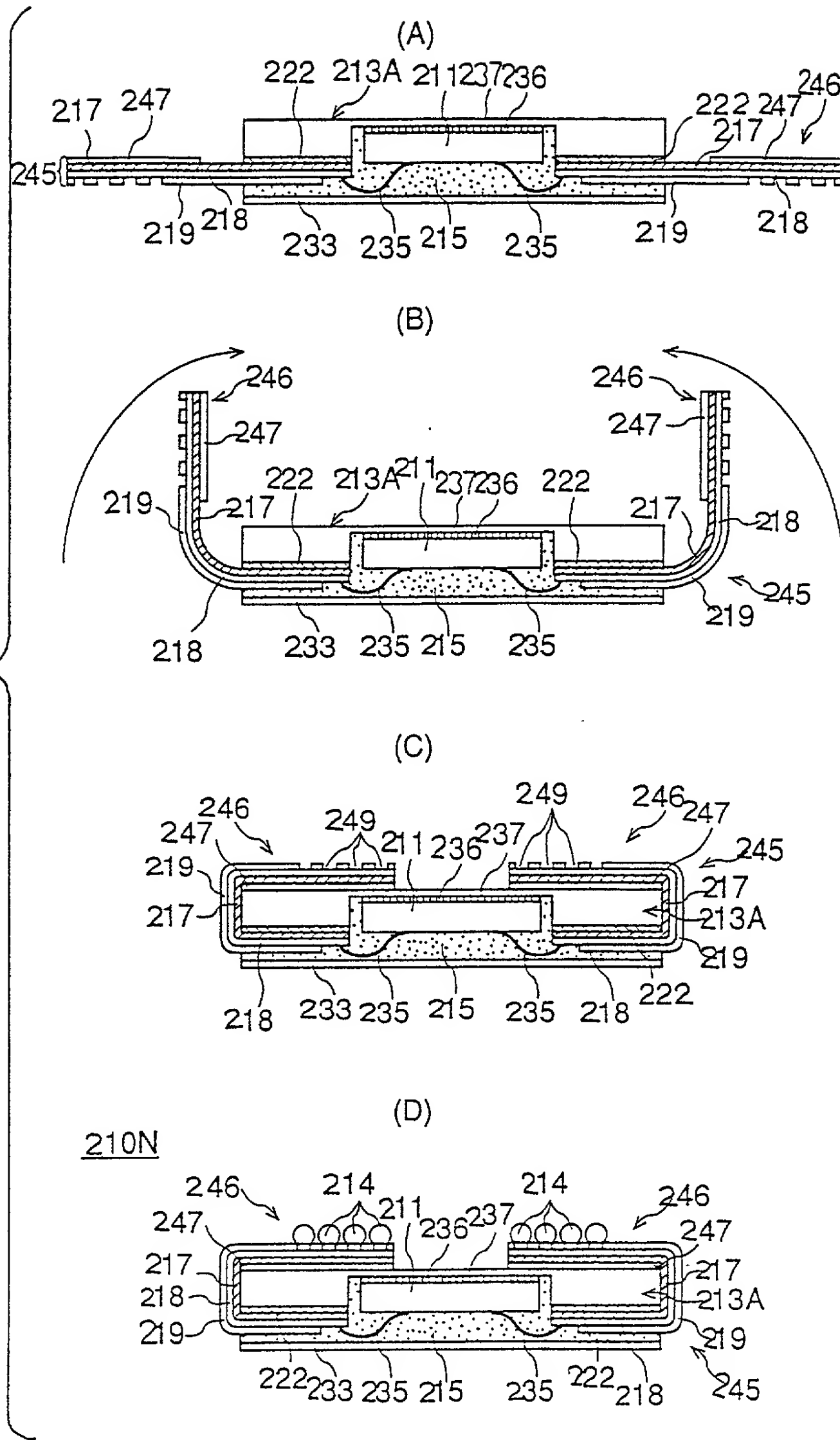


図 95





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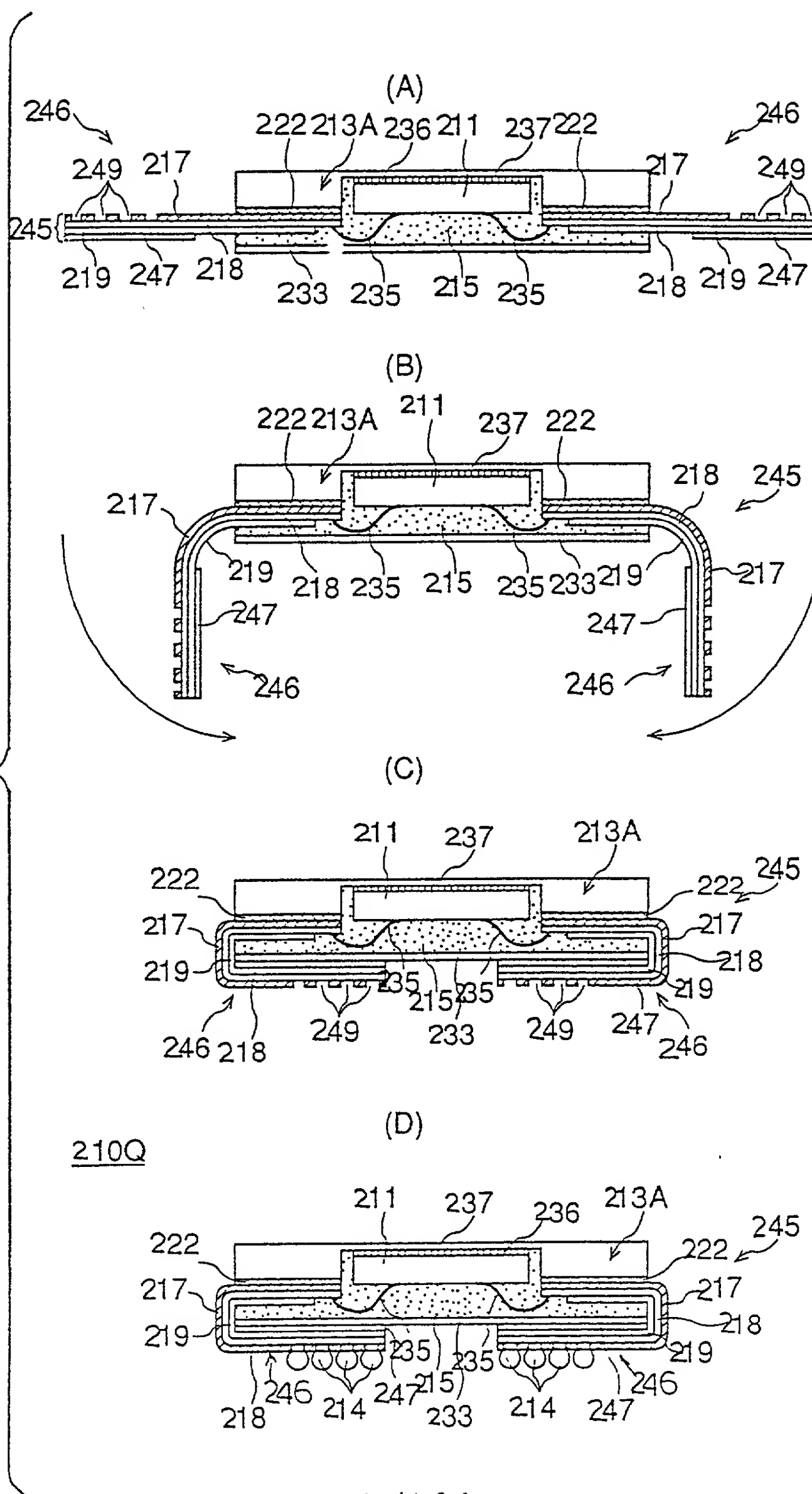
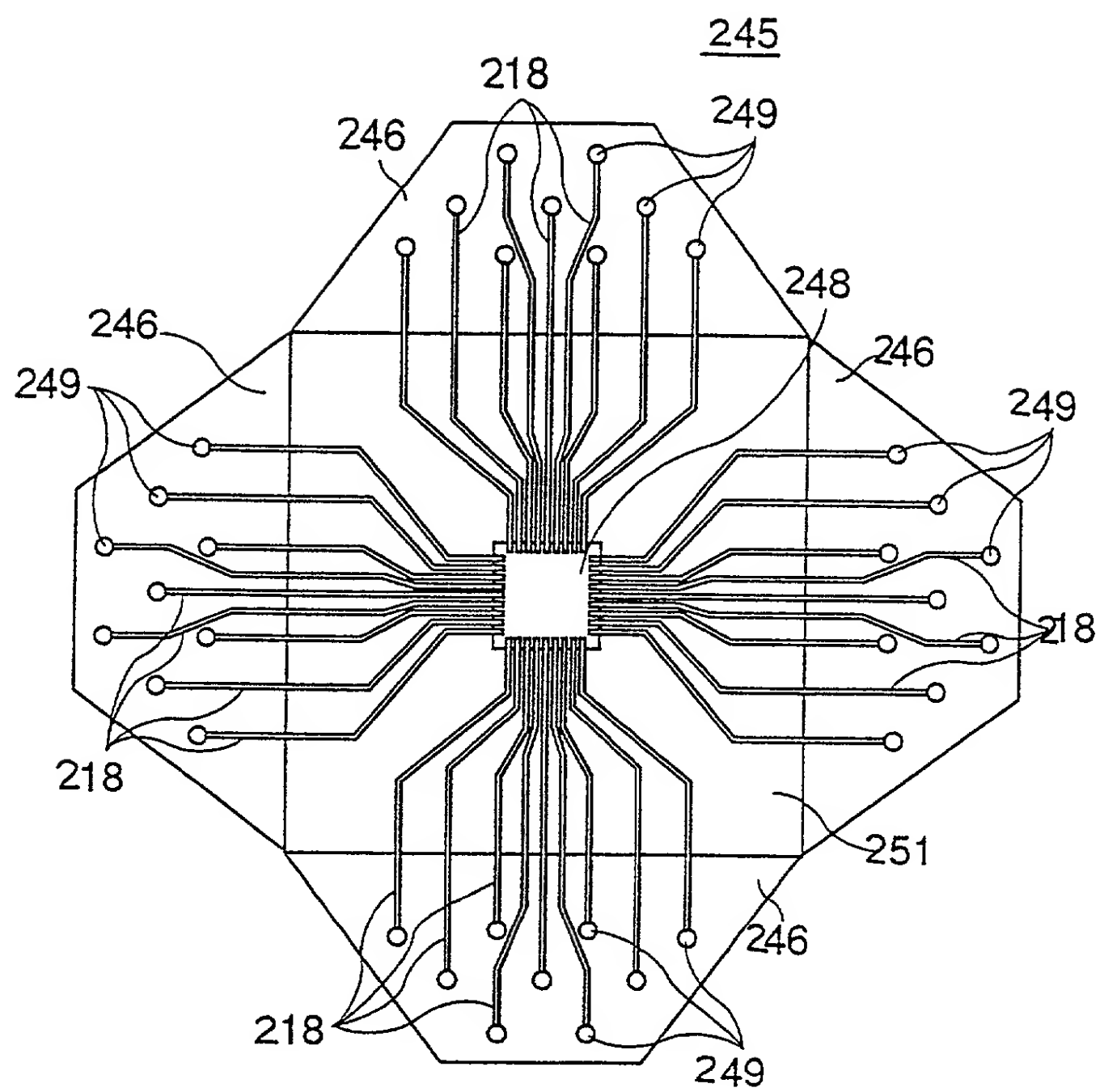


图 103



104

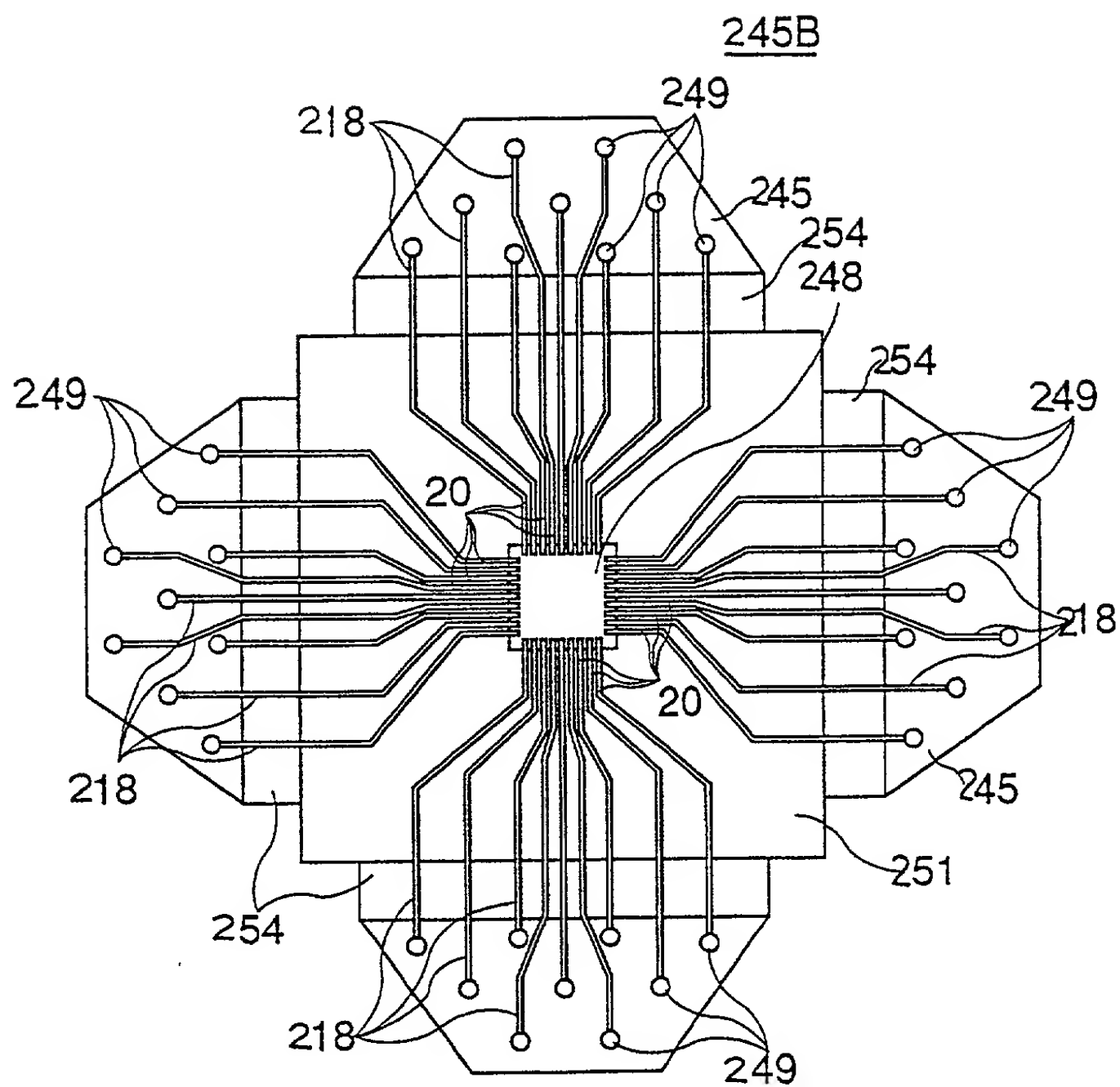


图 106

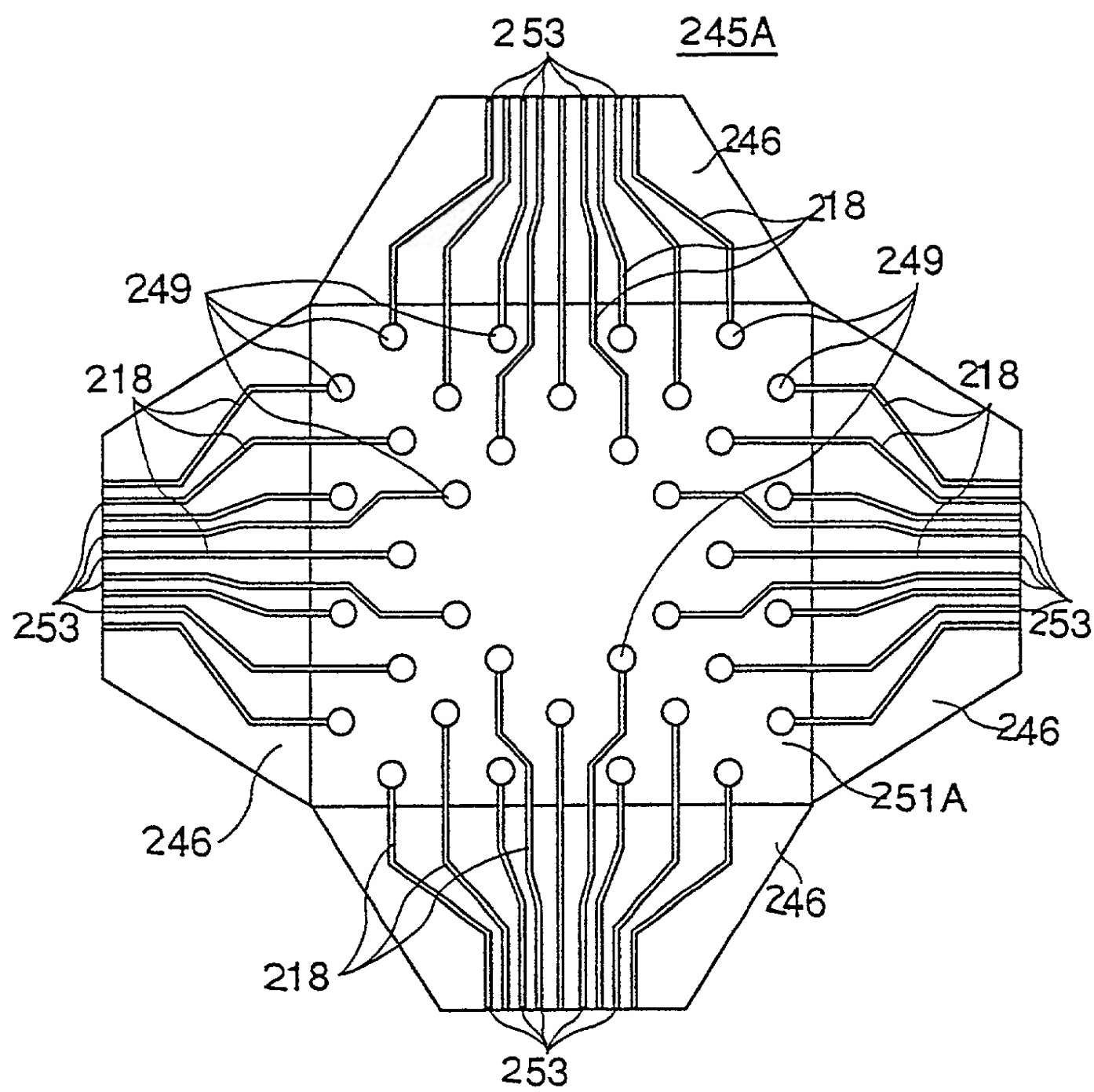


図 108

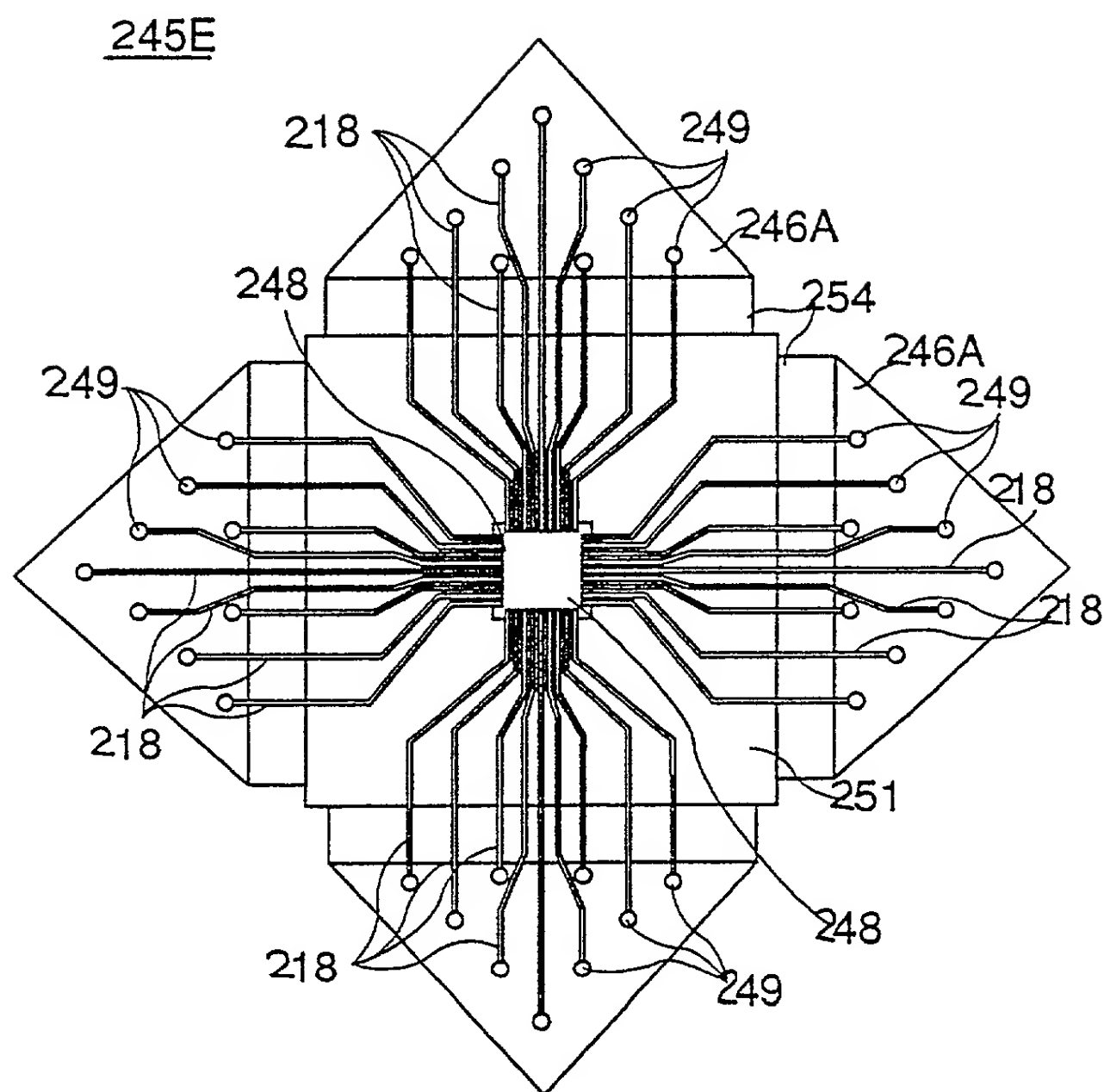
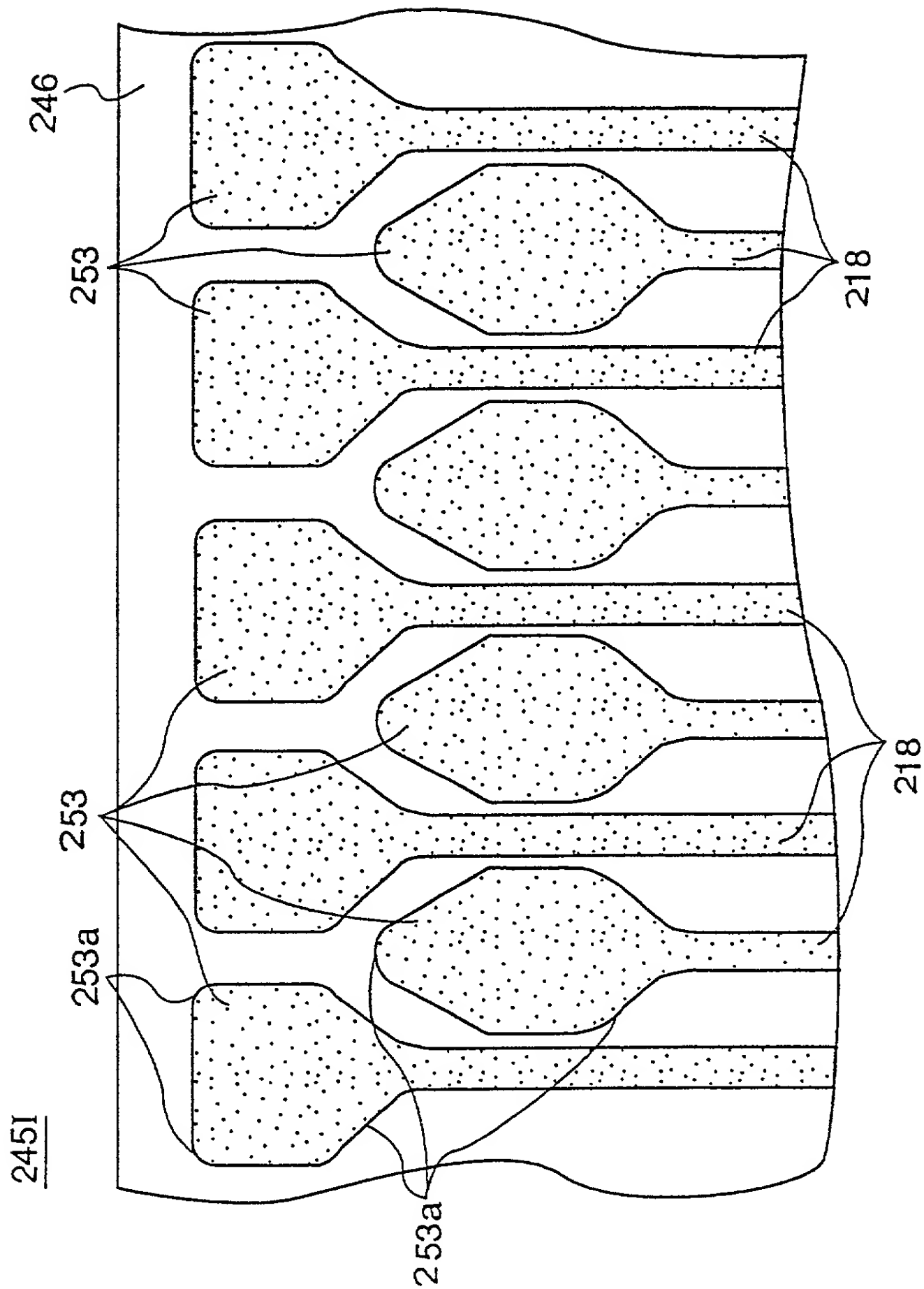


FIG. 110



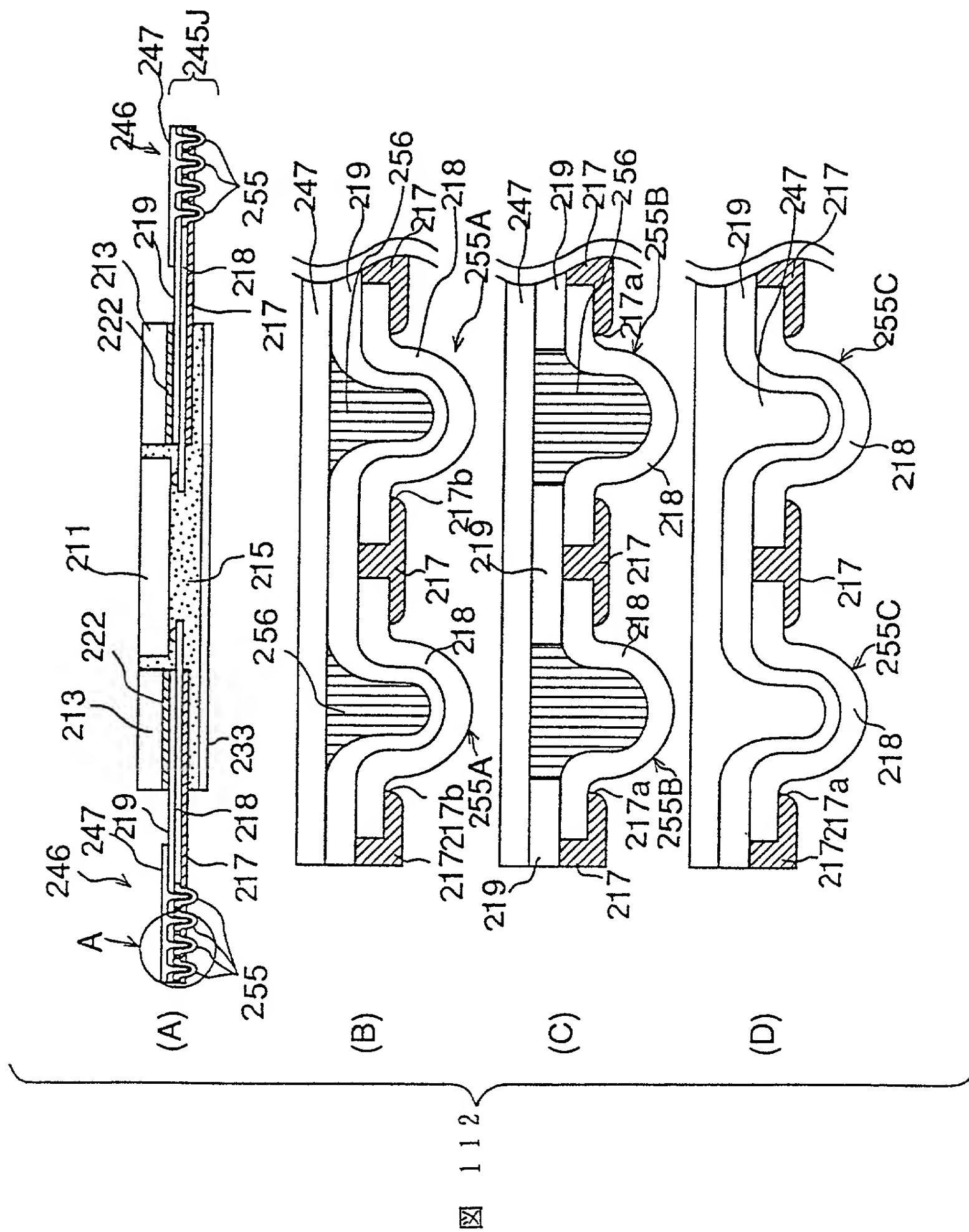


図 114

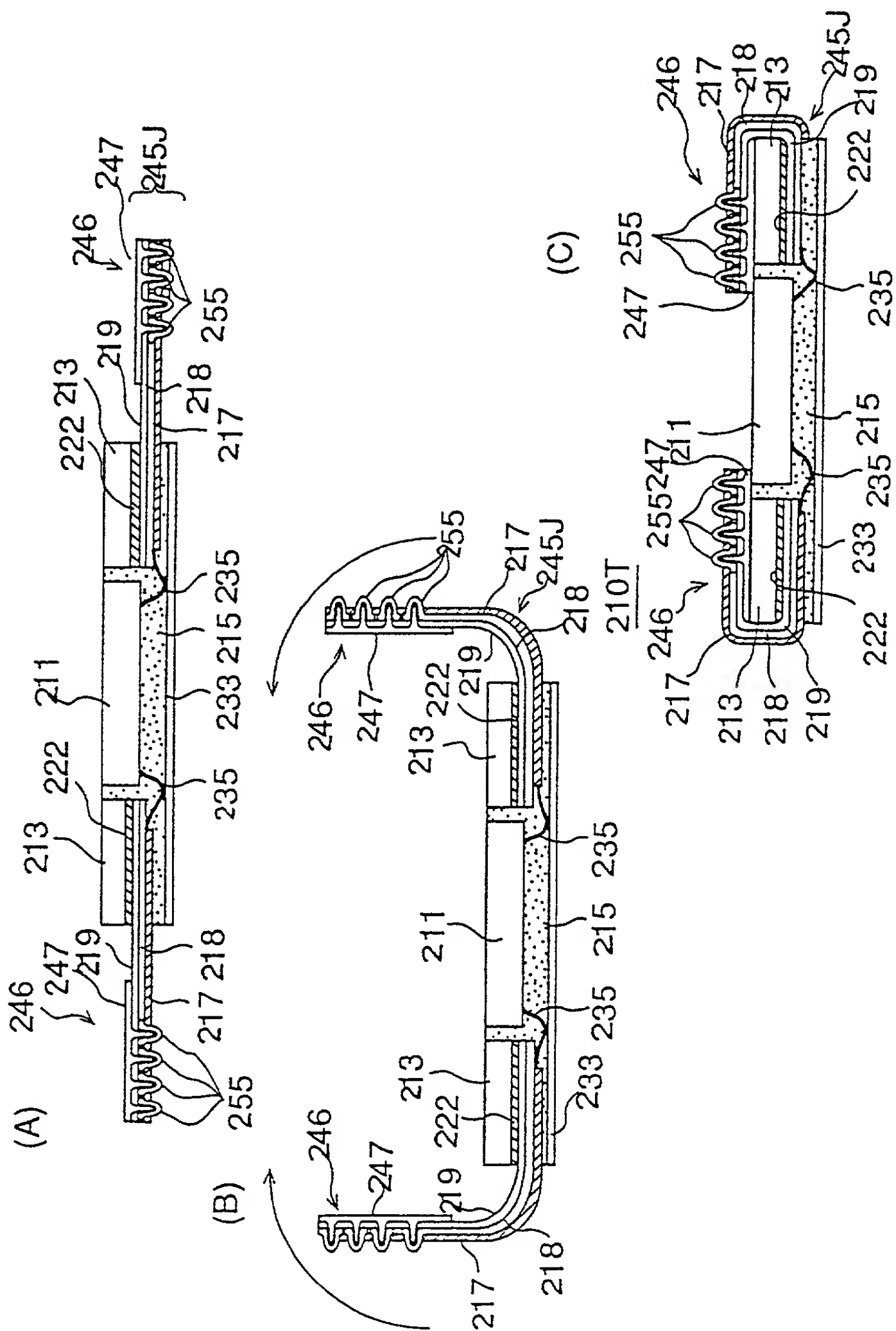
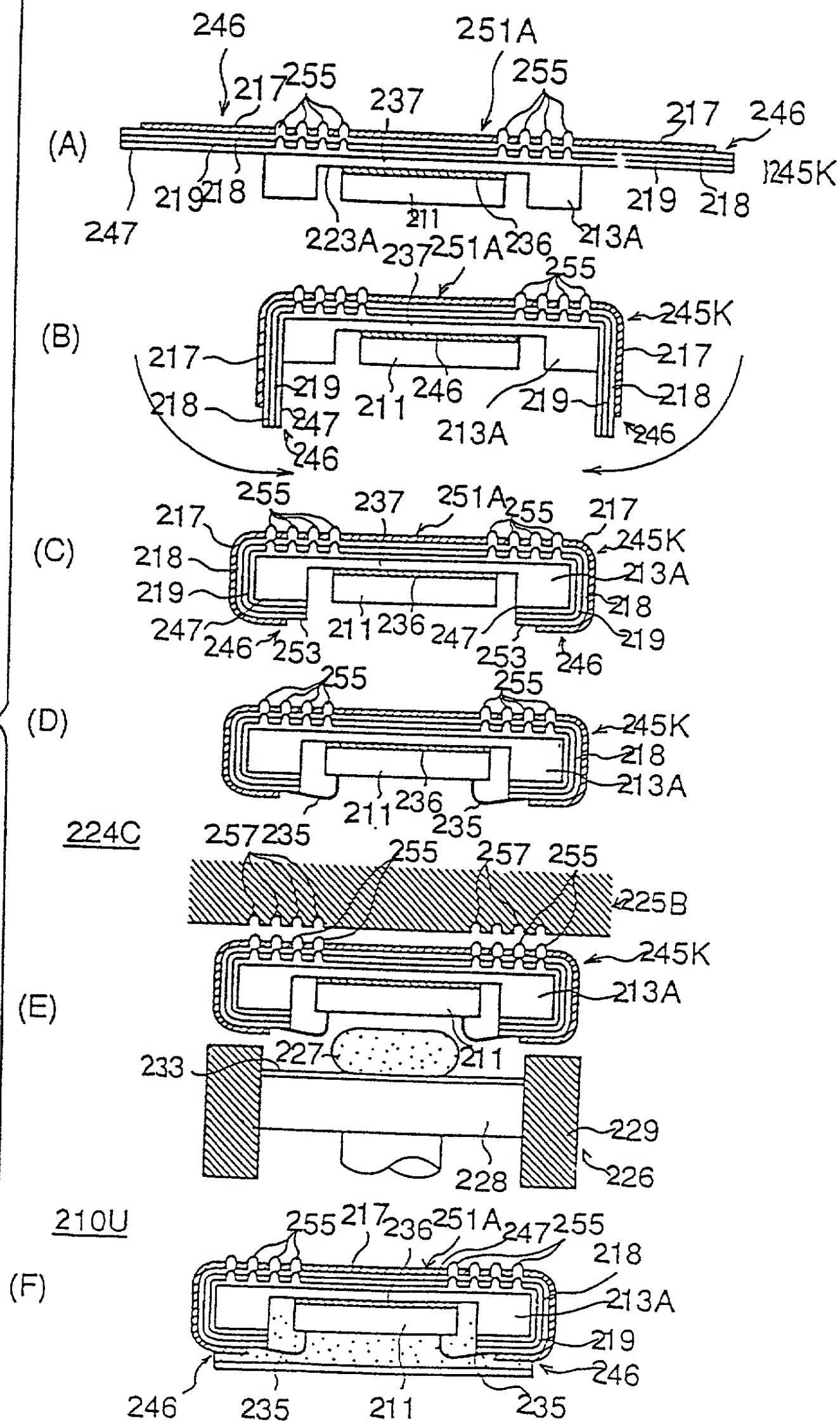
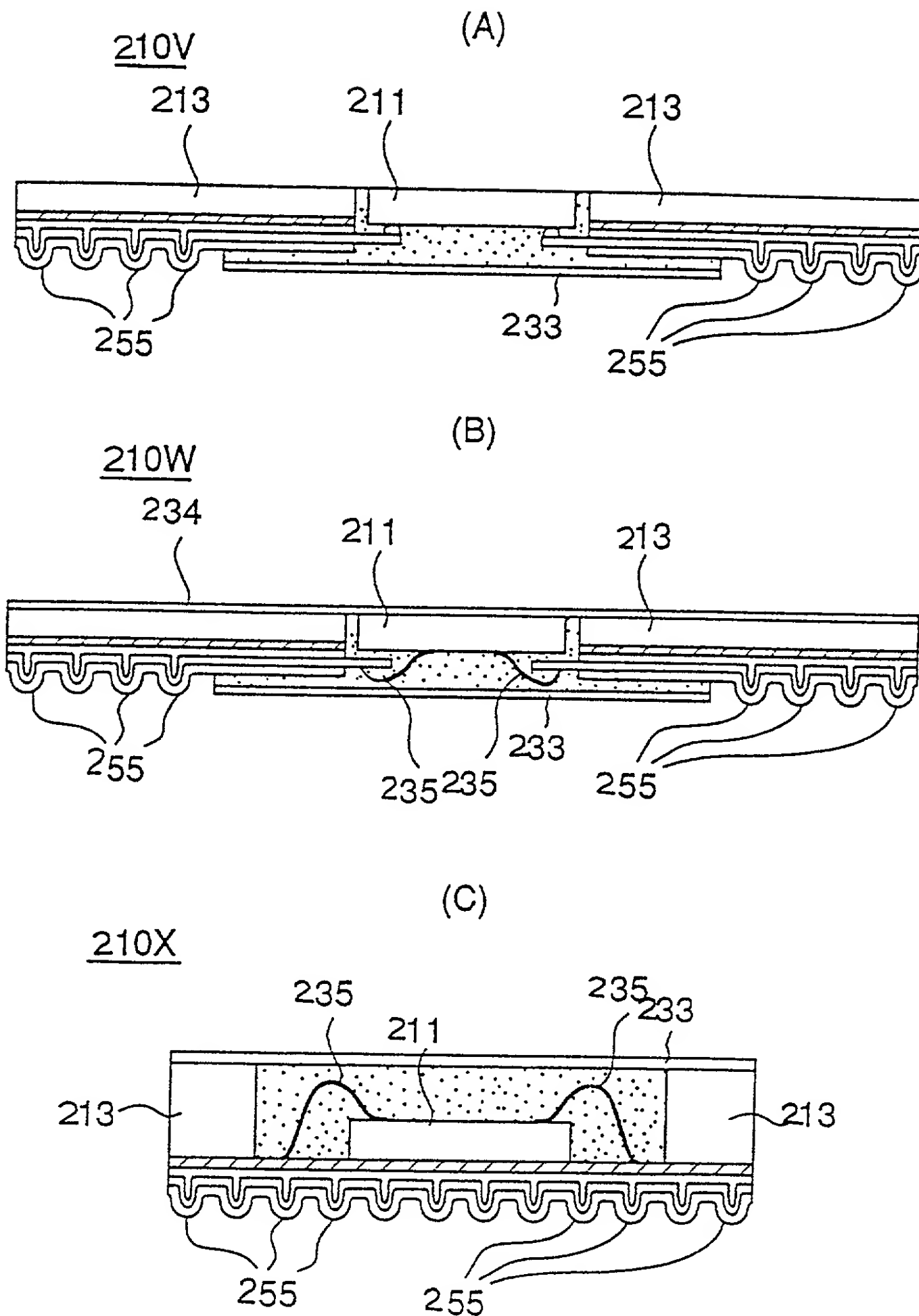


図 115



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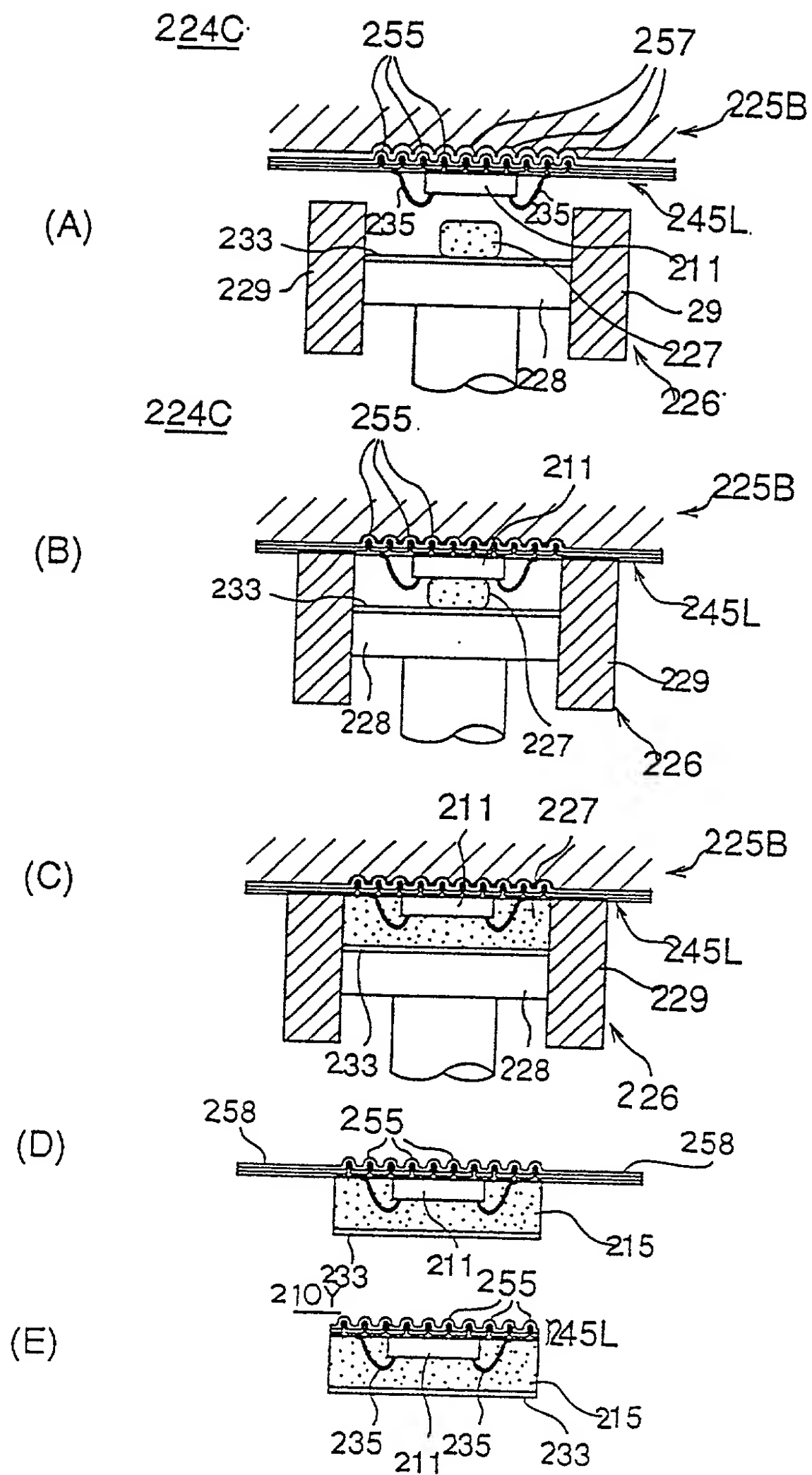
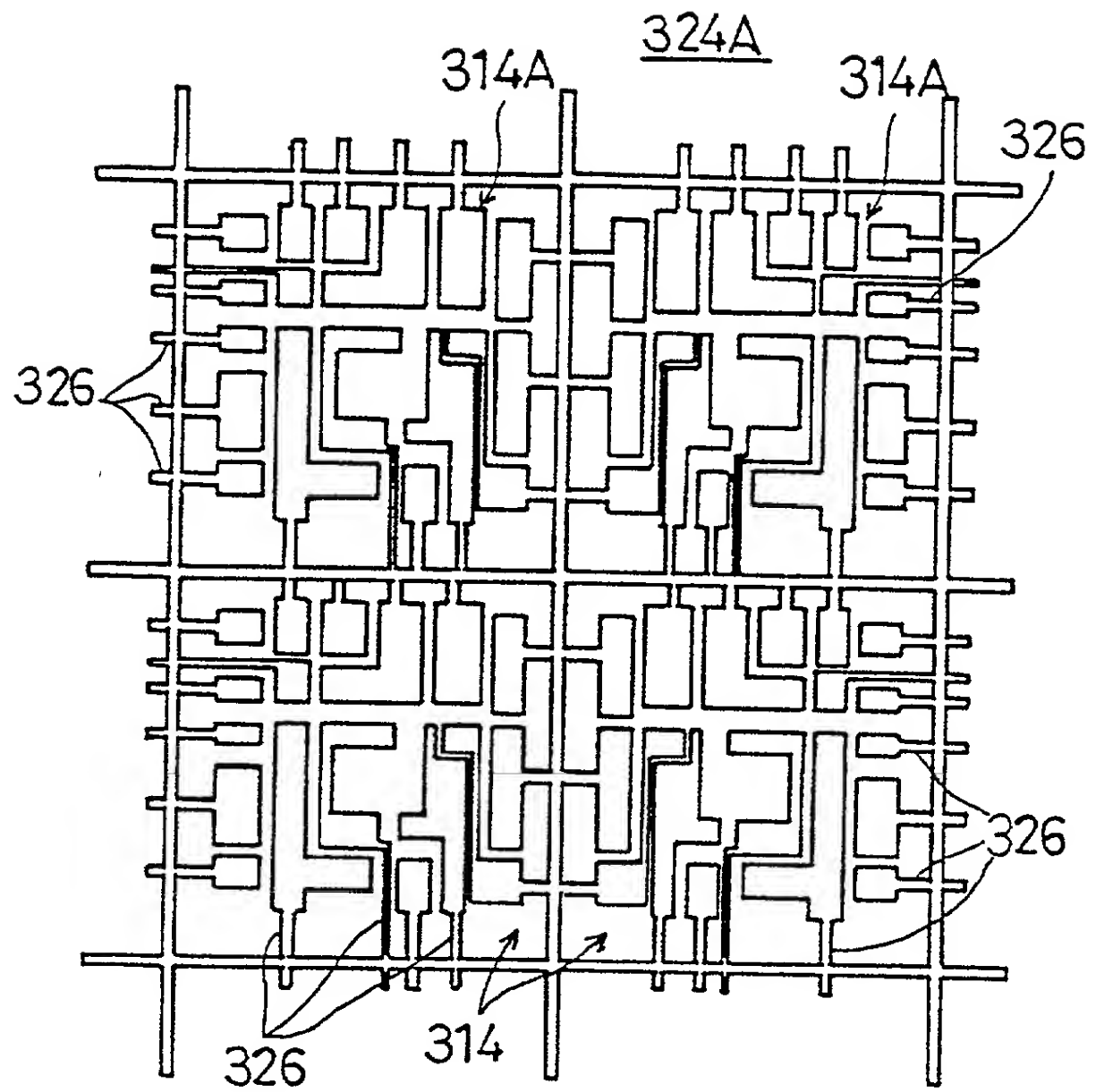


図 119

(A)



(B)

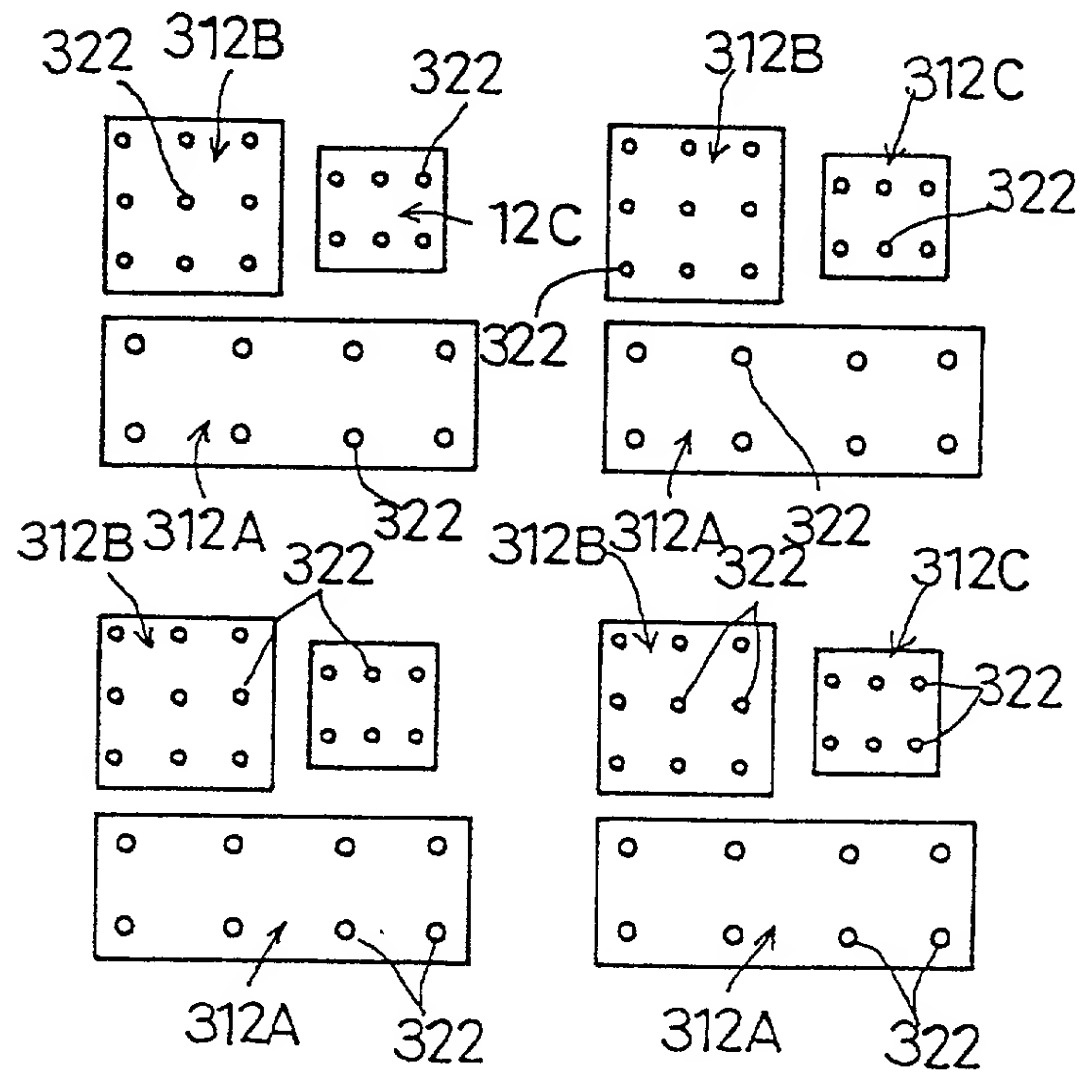


図 123

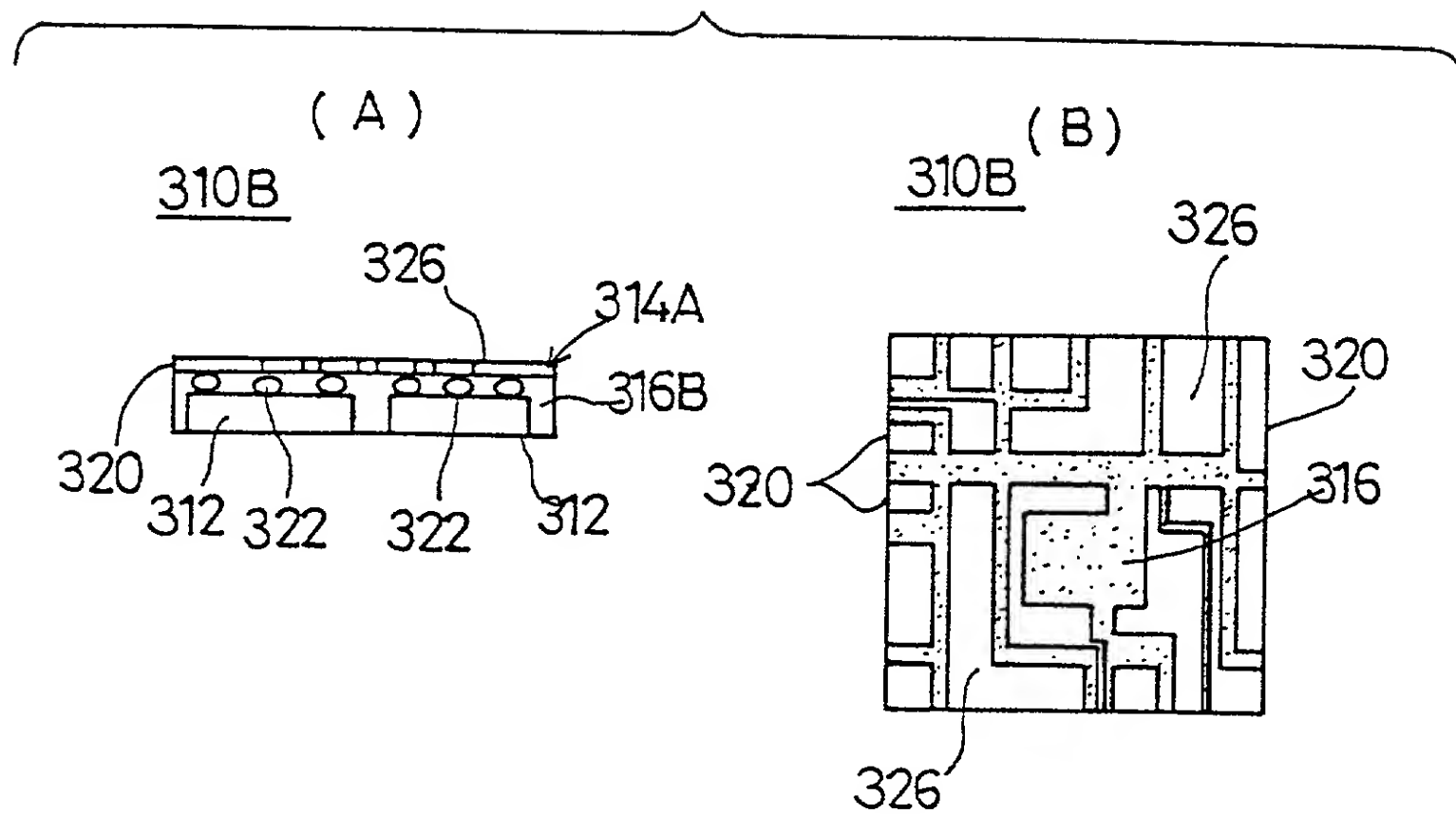


図 124

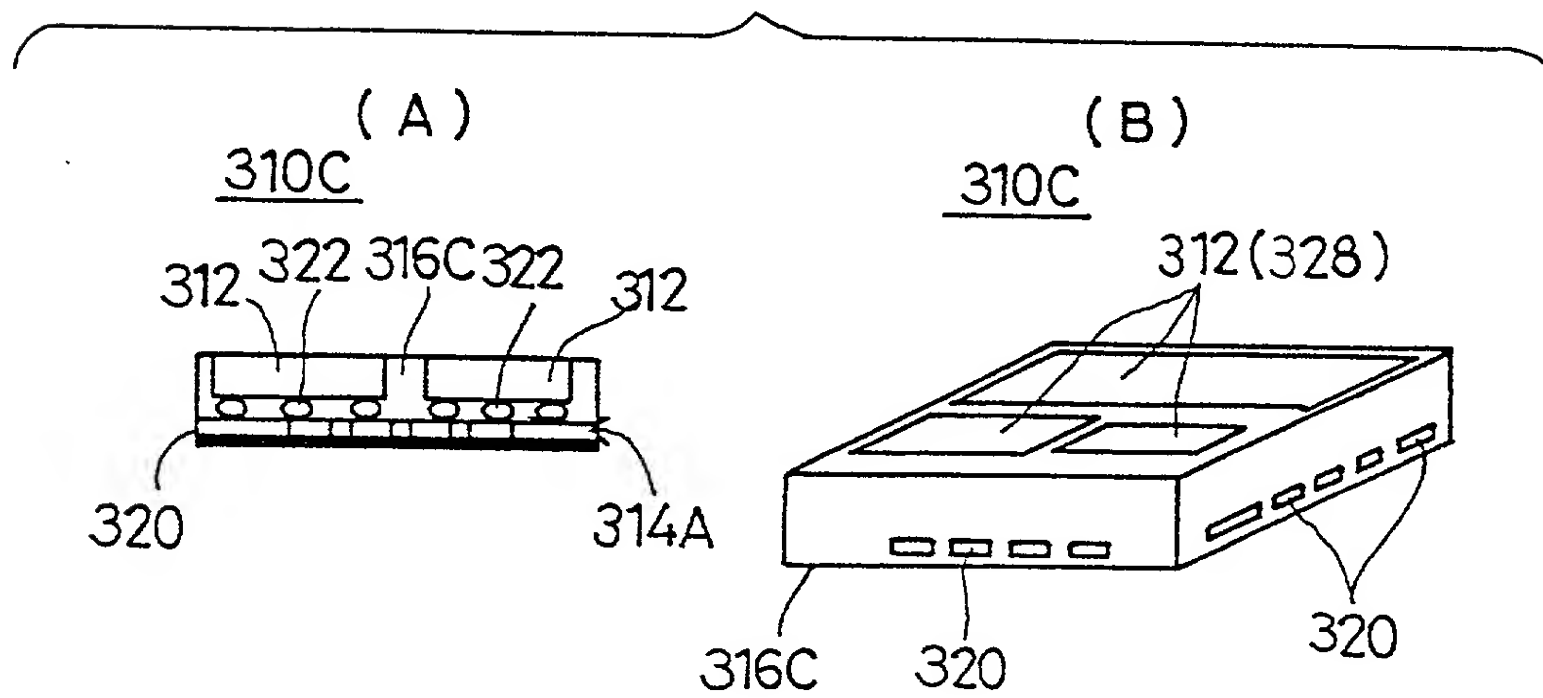


FIG. 126

324B

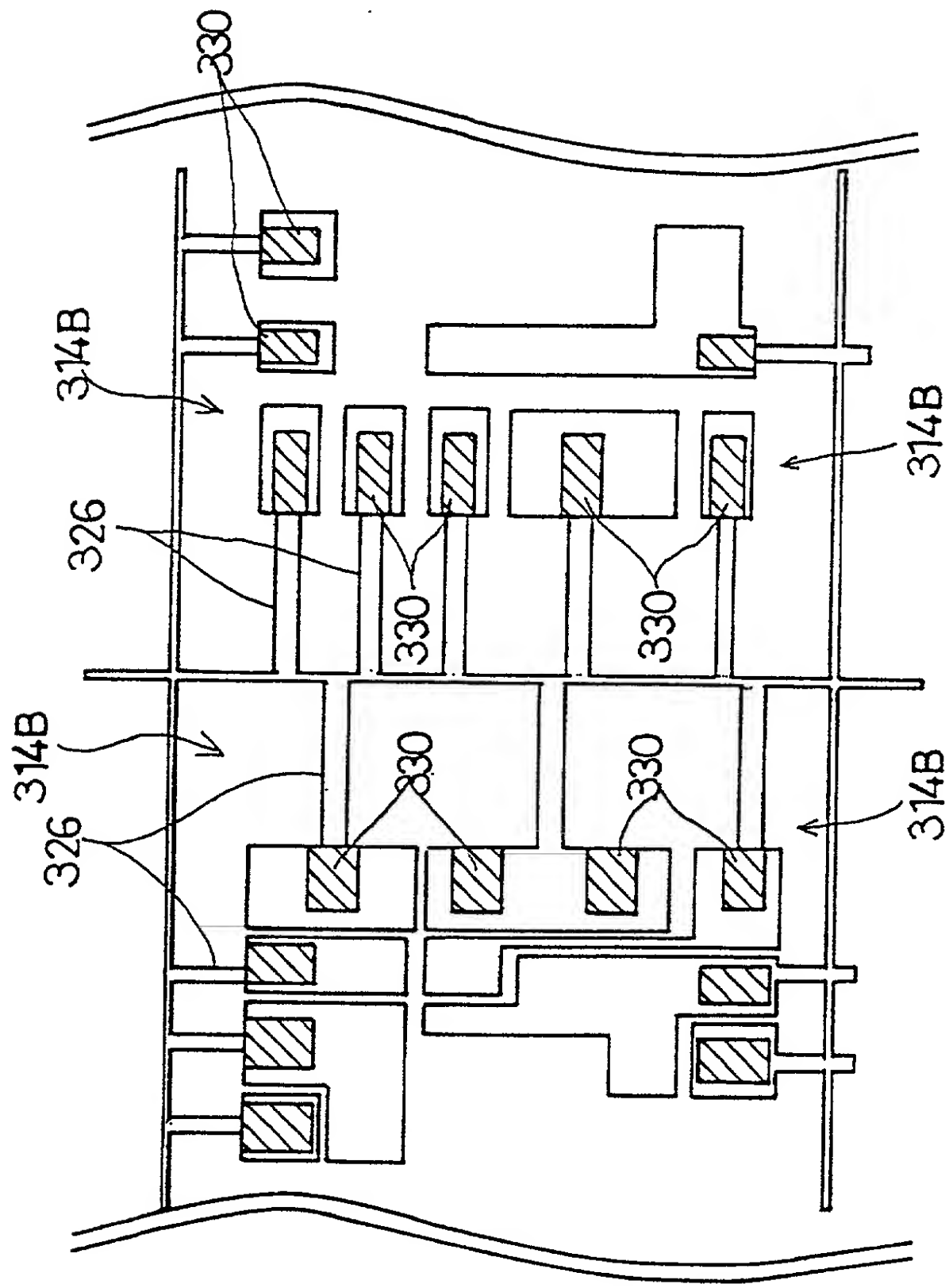


图 128

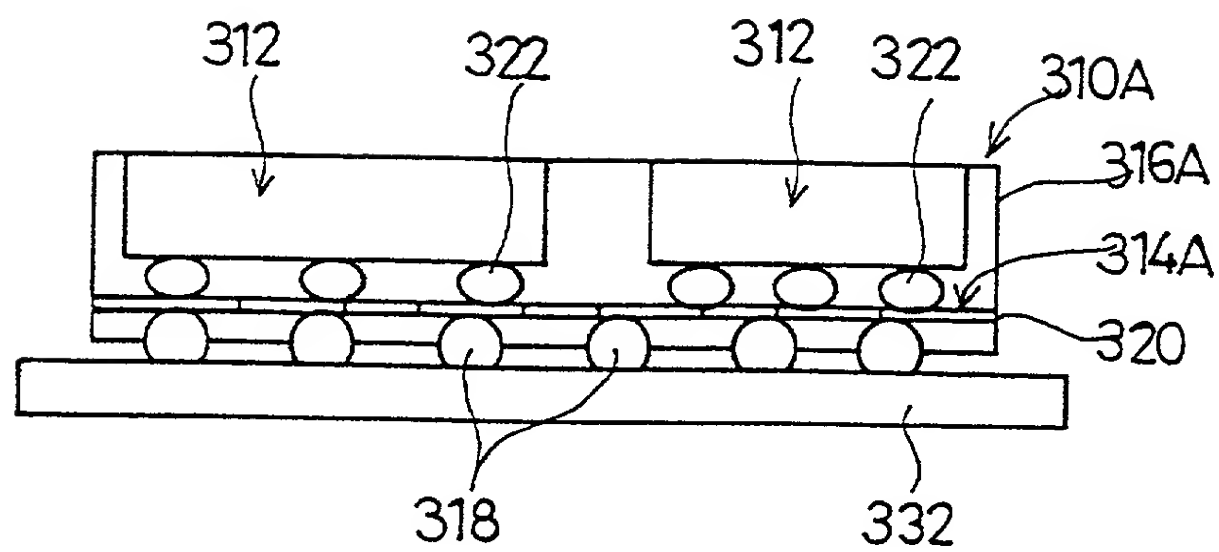


图 129

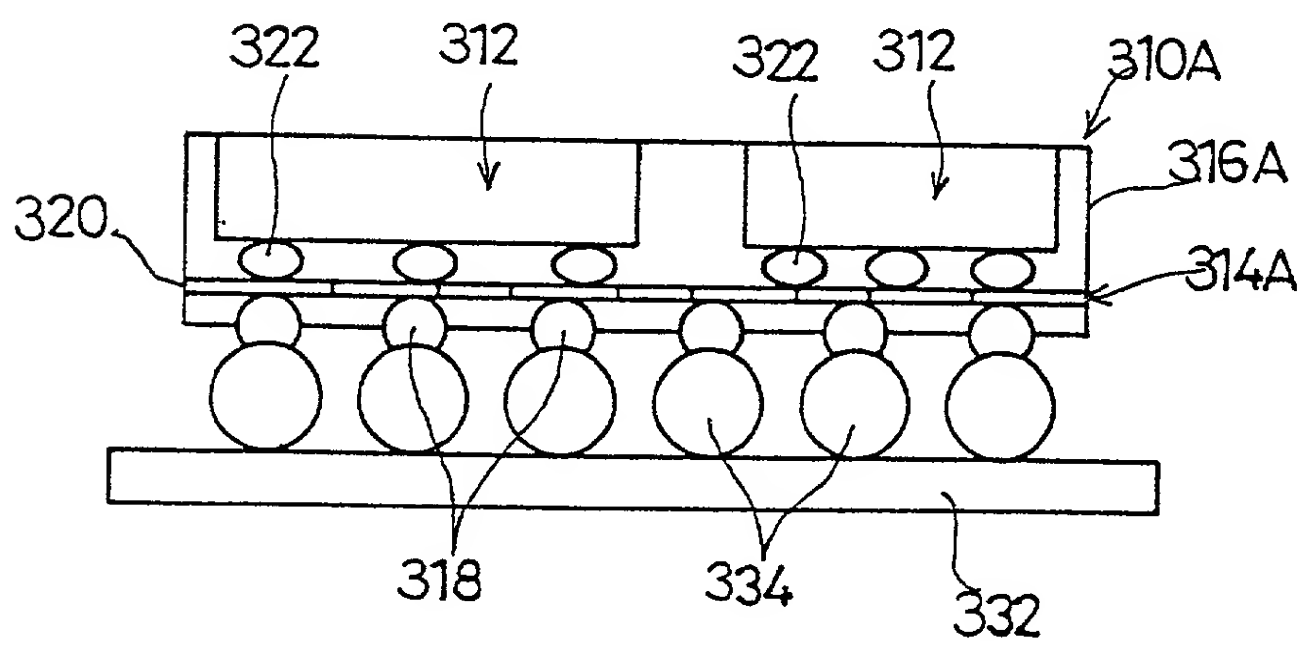


図 132

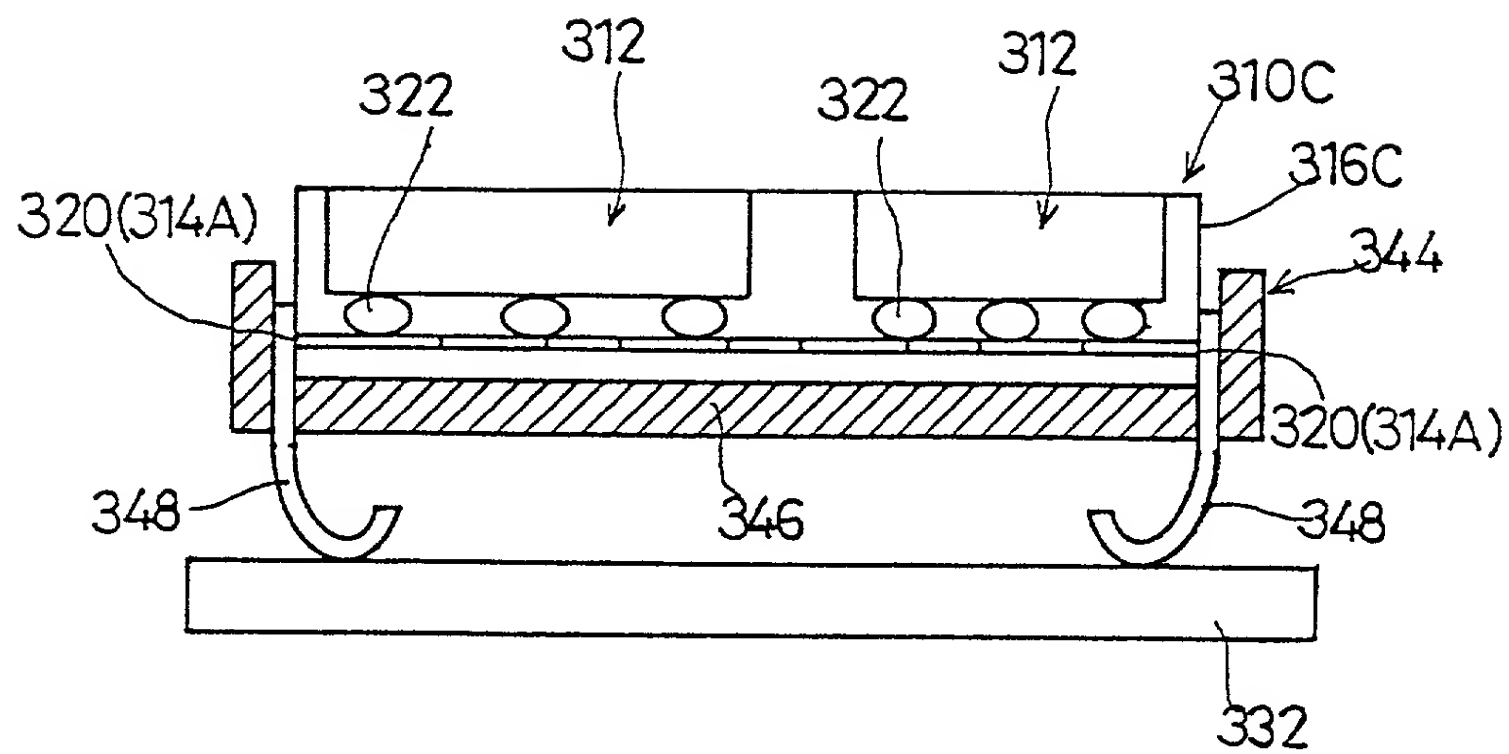
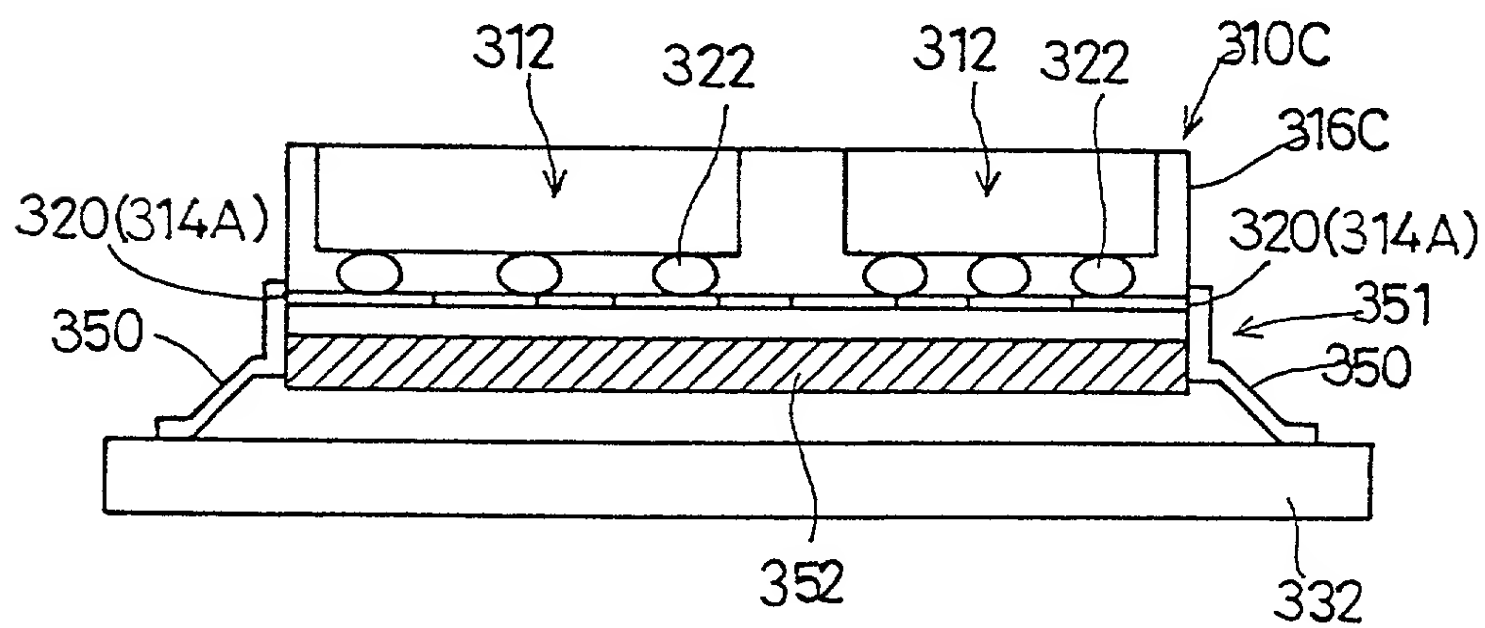


図 133



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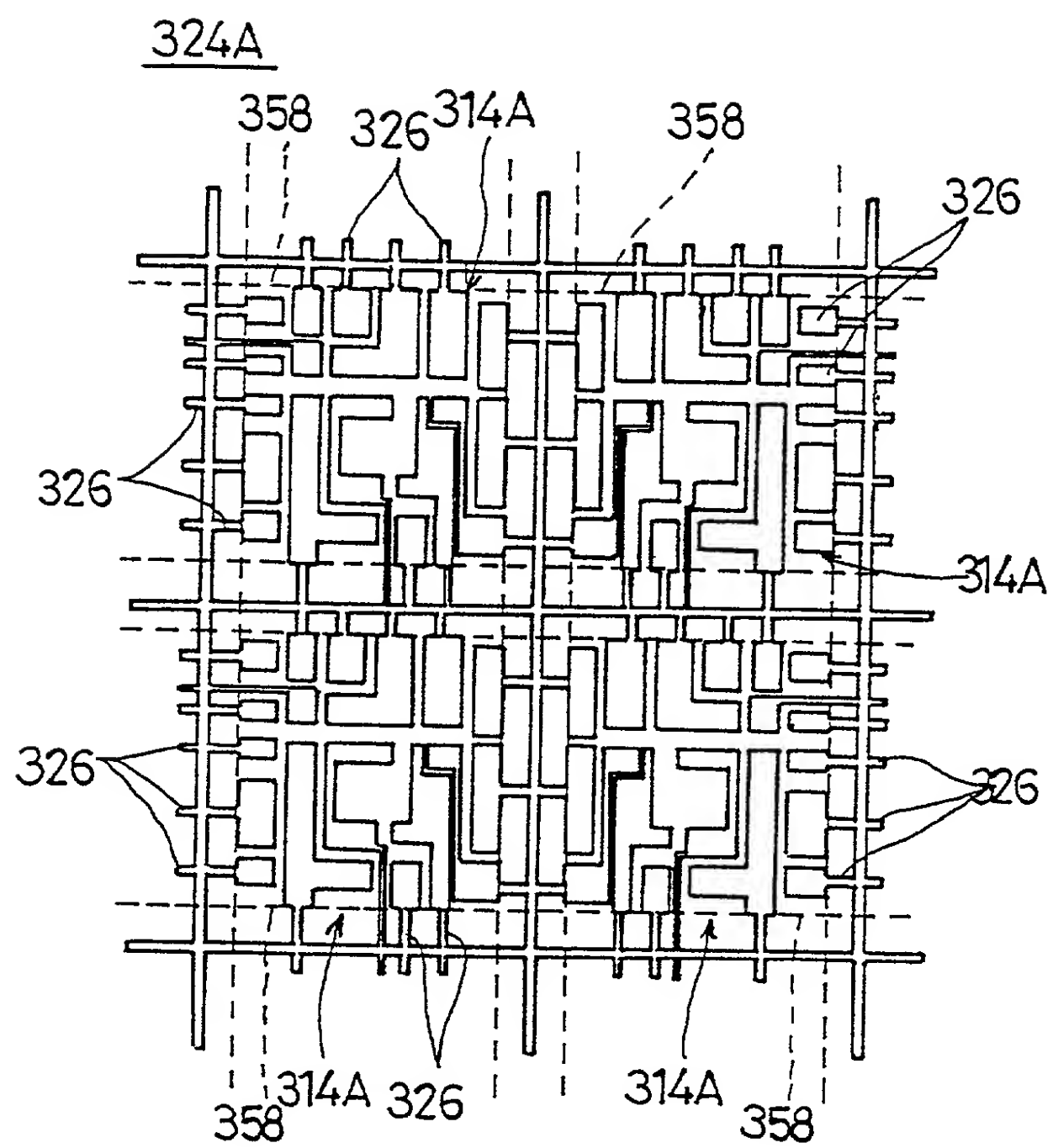


図 139

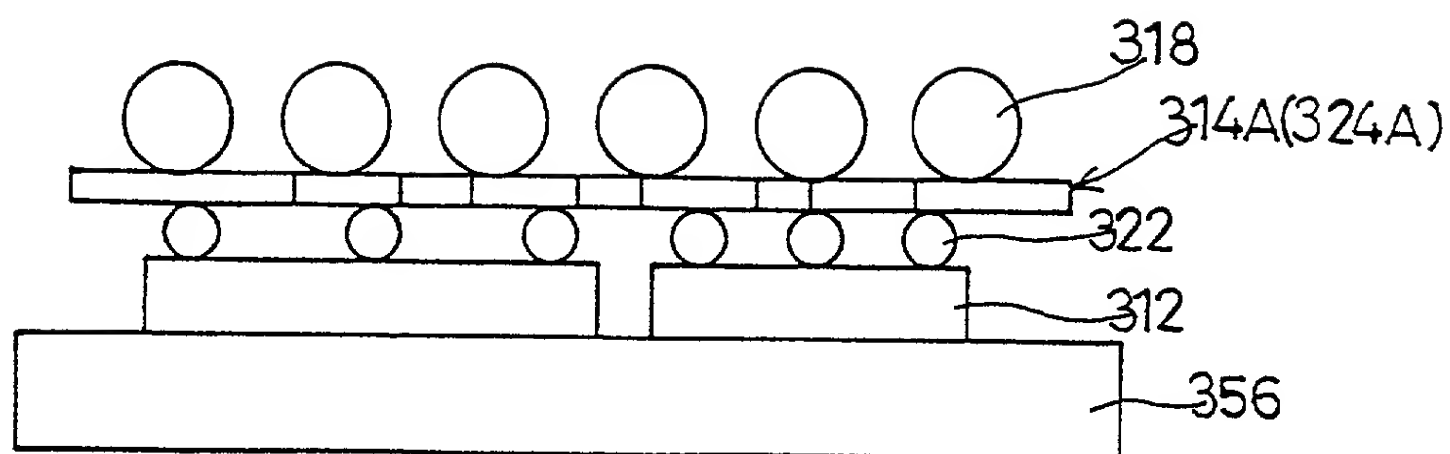


図 140

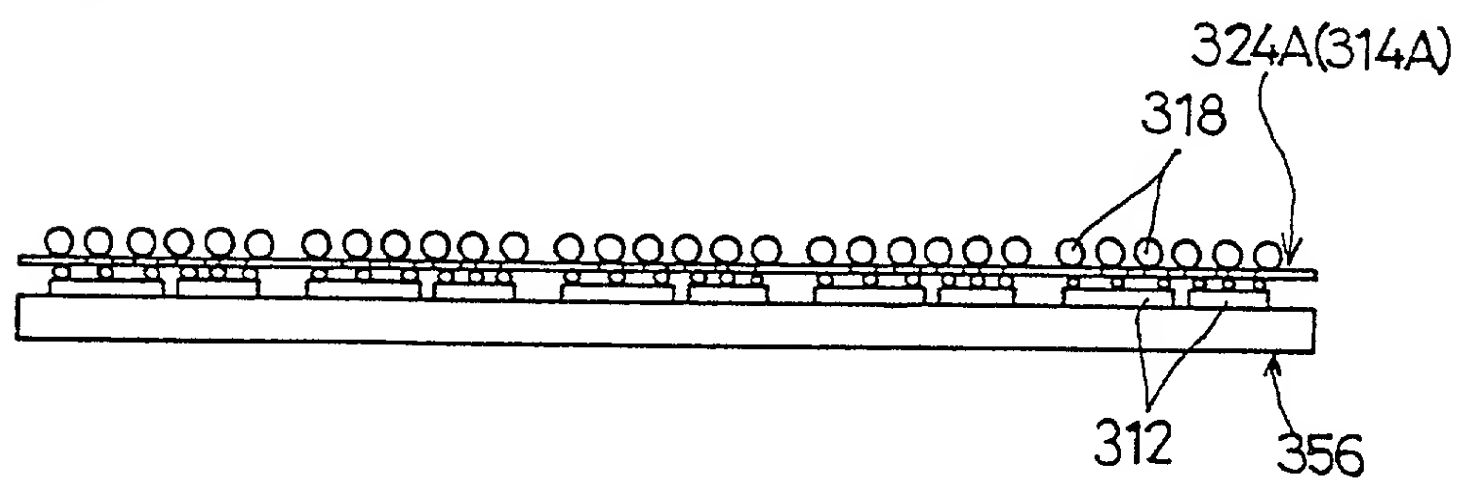


図 141

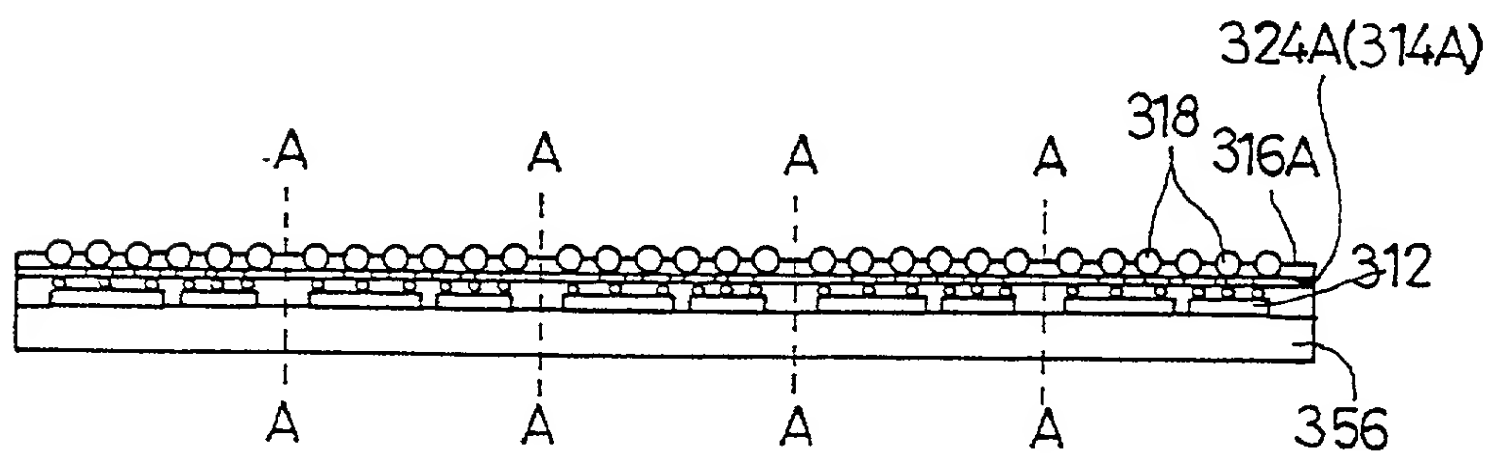


図 143

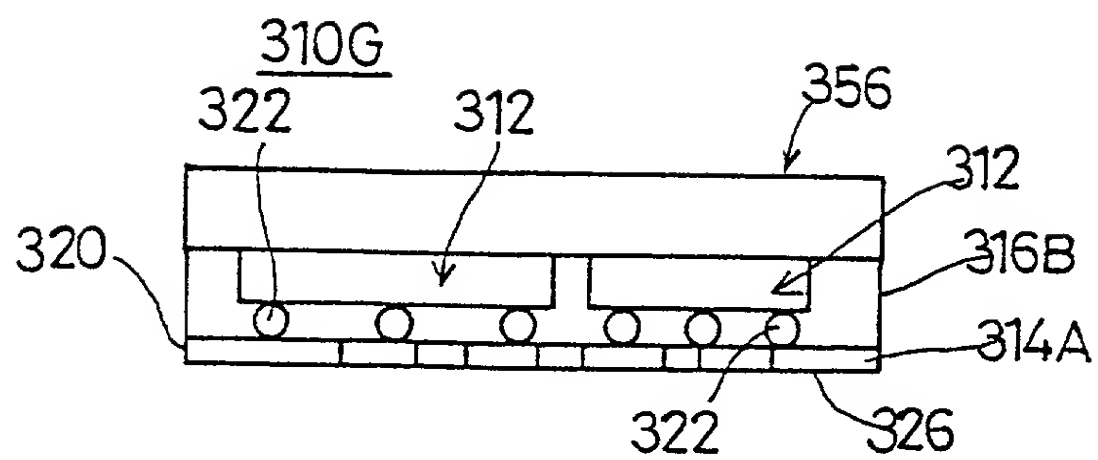


図 144

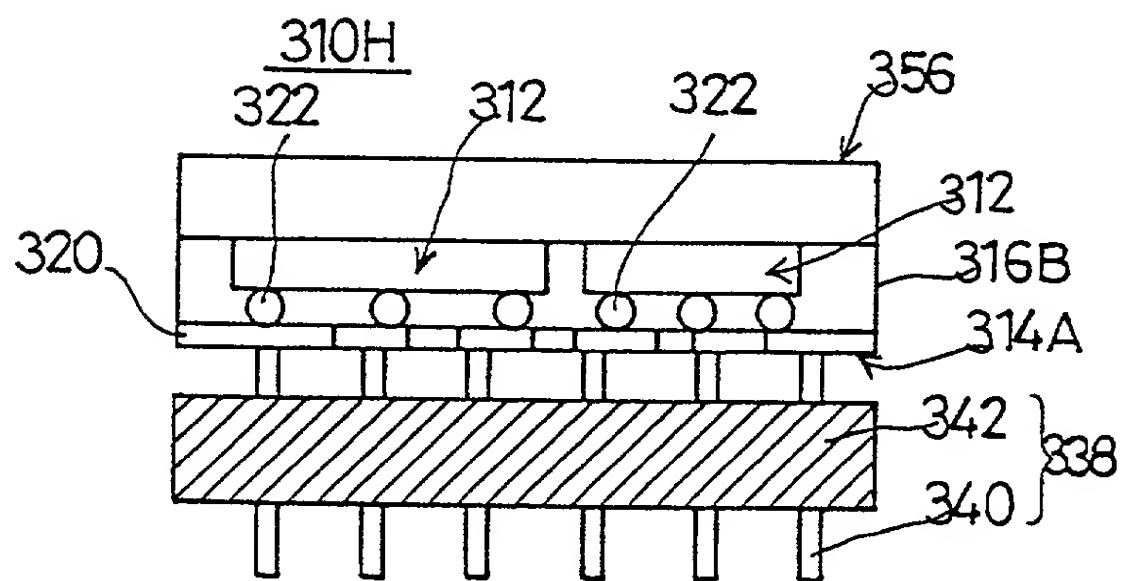


図 145

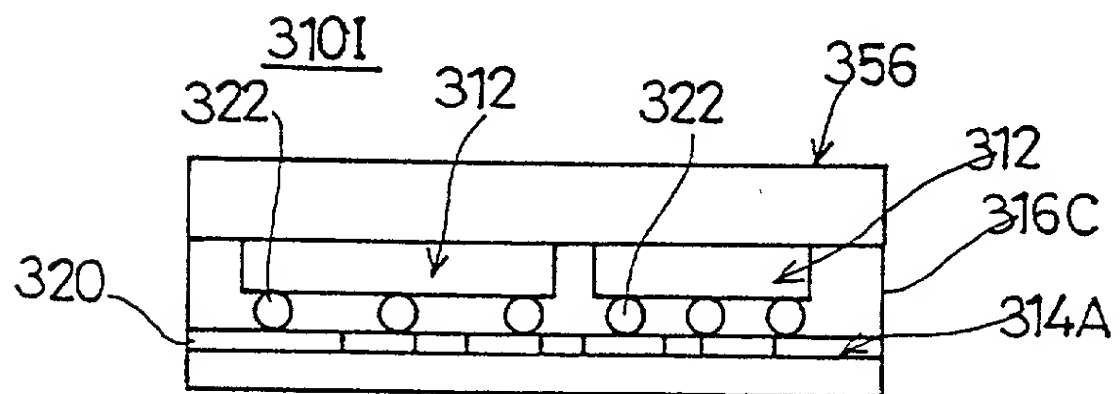


図 151

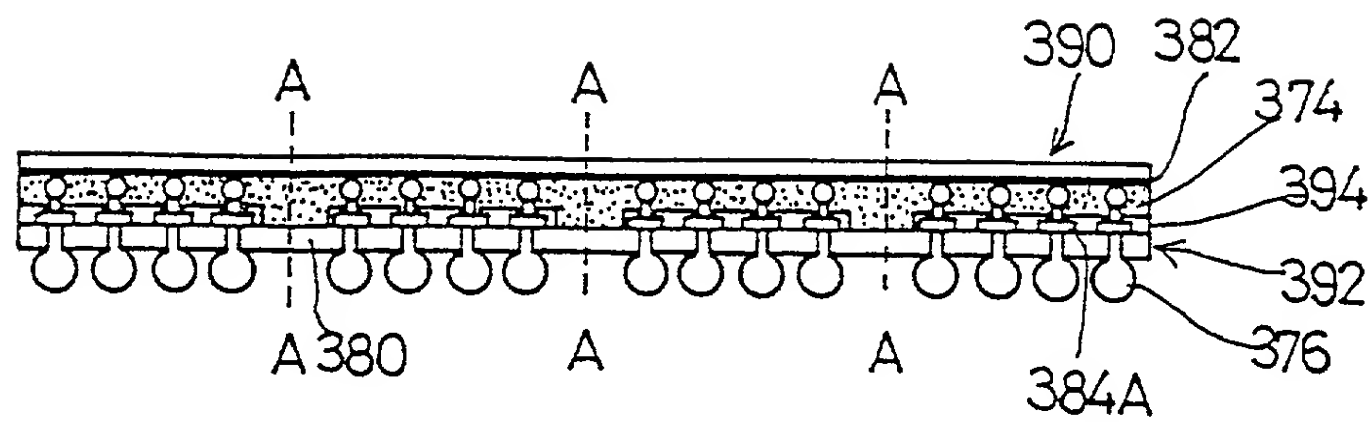


図 152

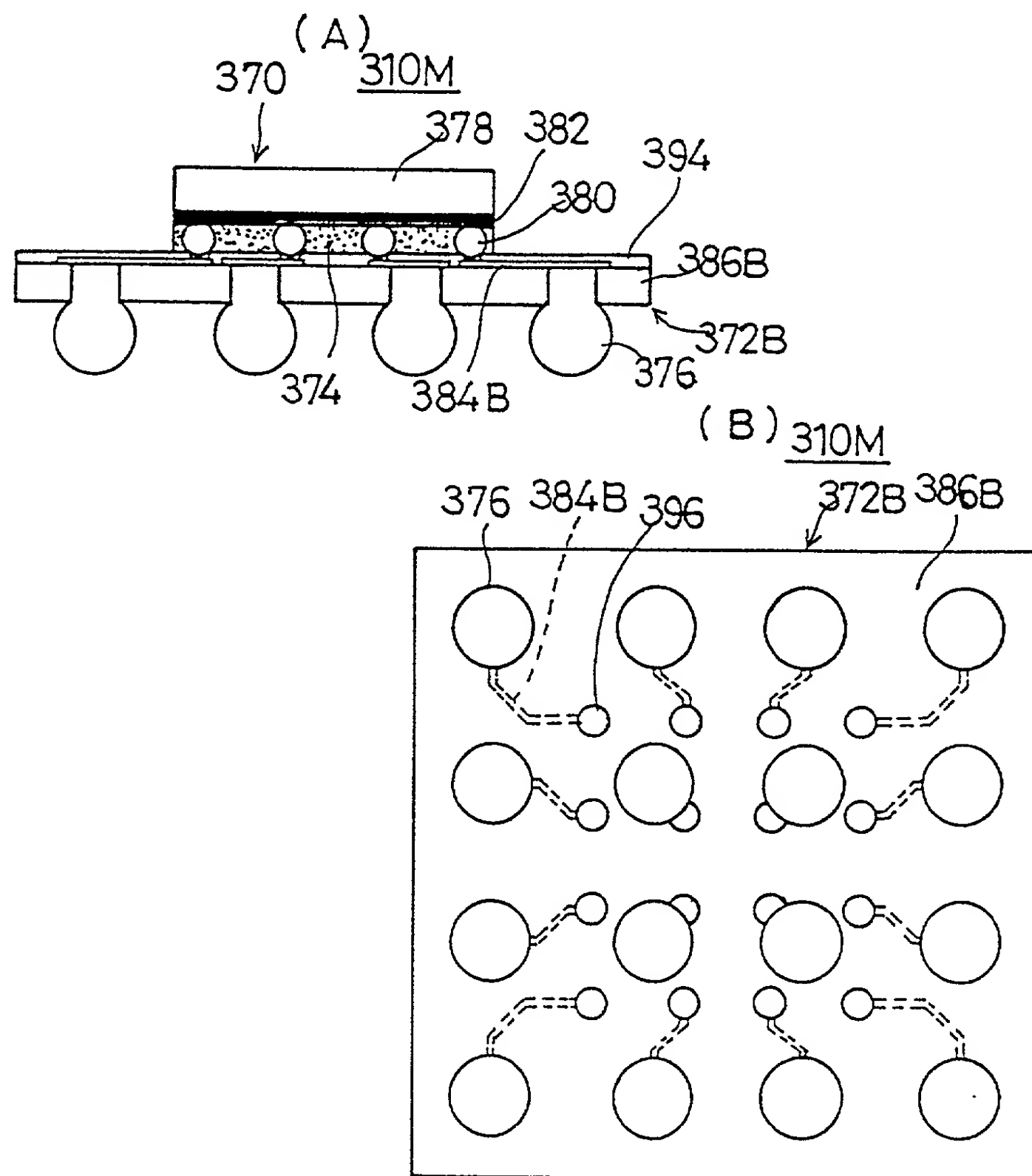


図 159

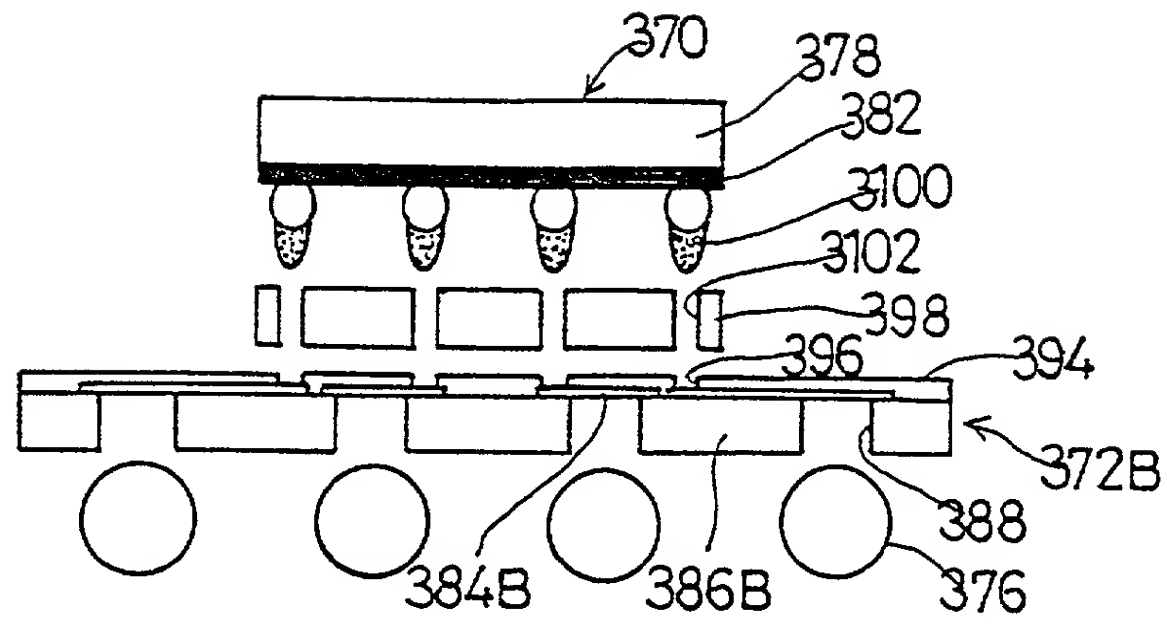


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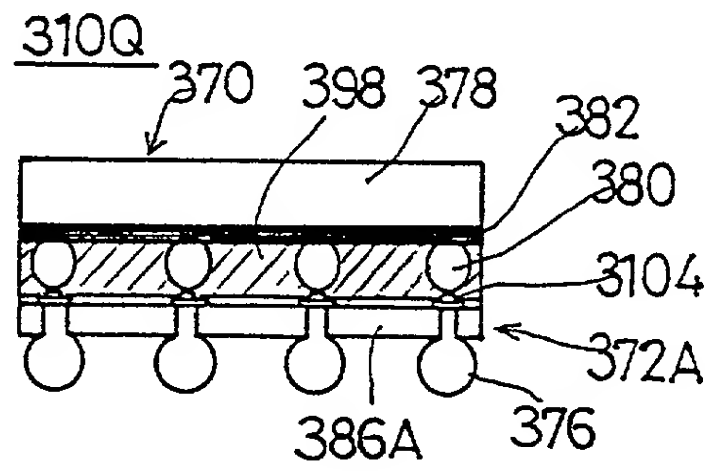


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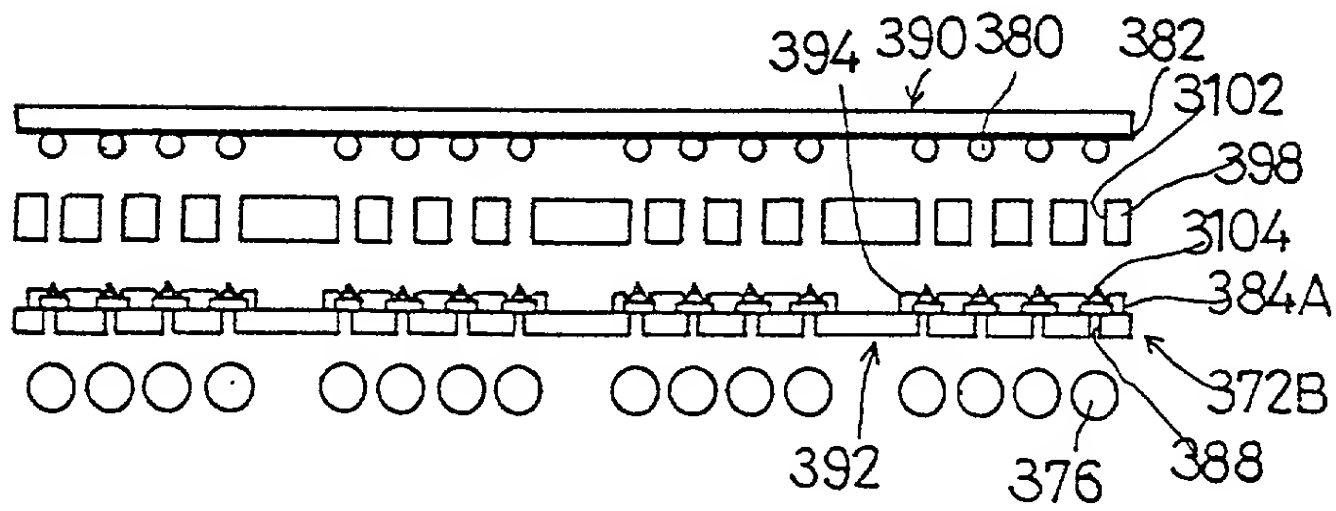


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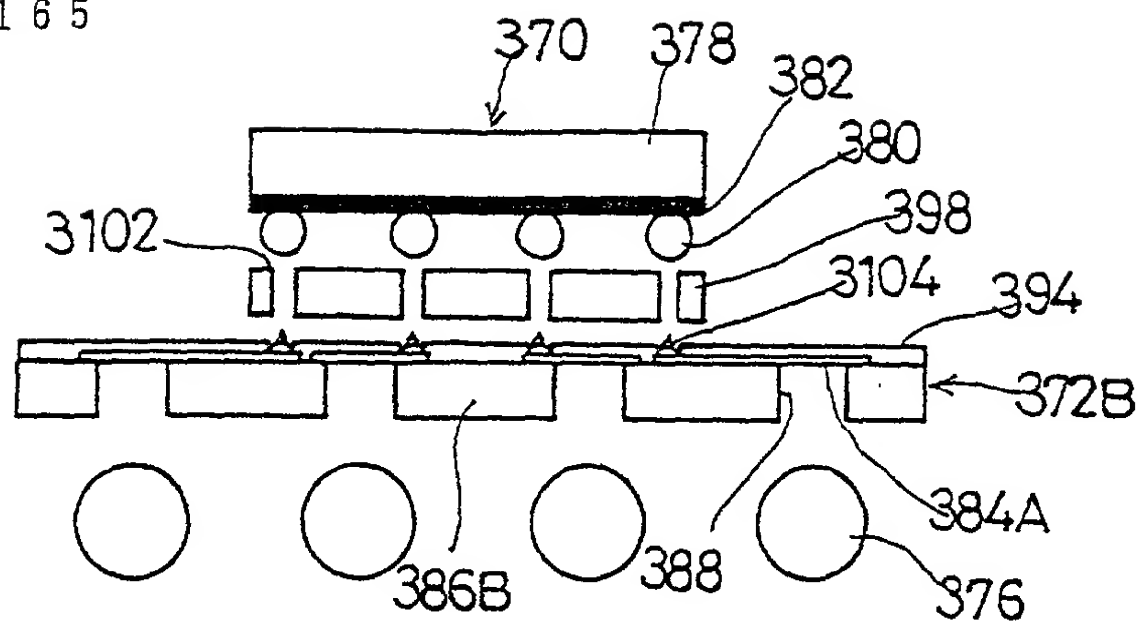


図 166

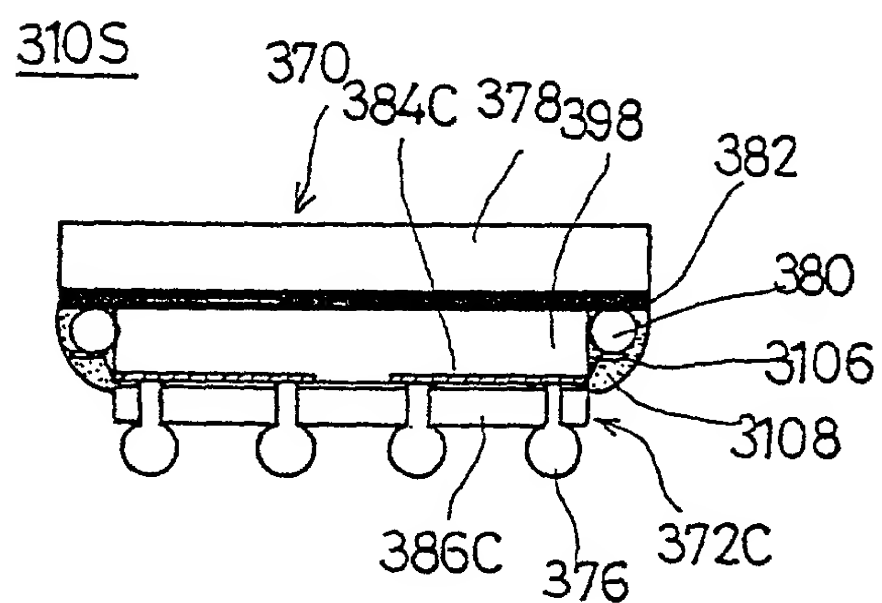


図 167

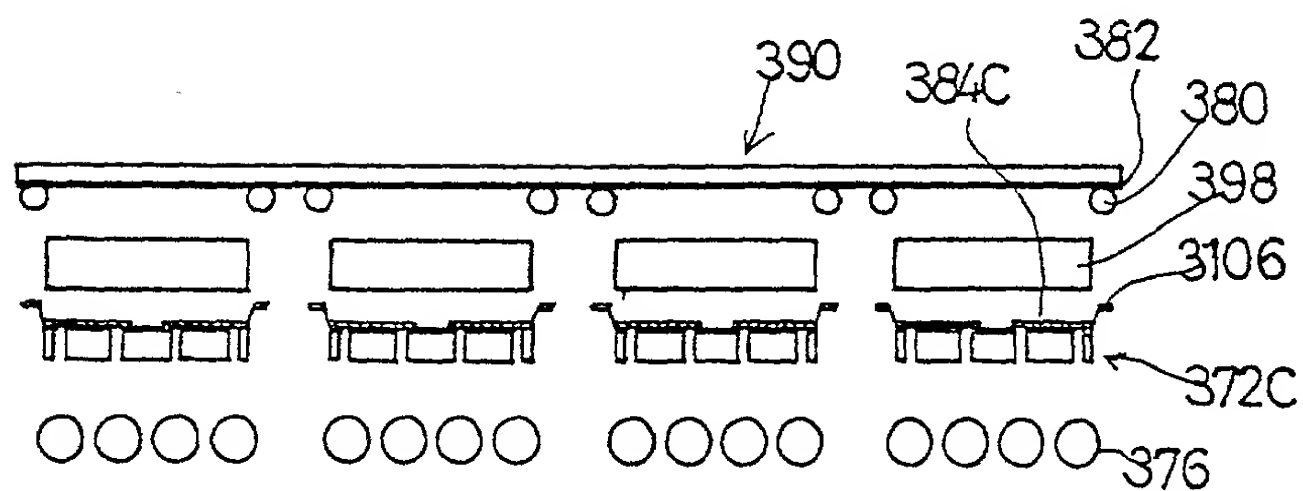


图 168

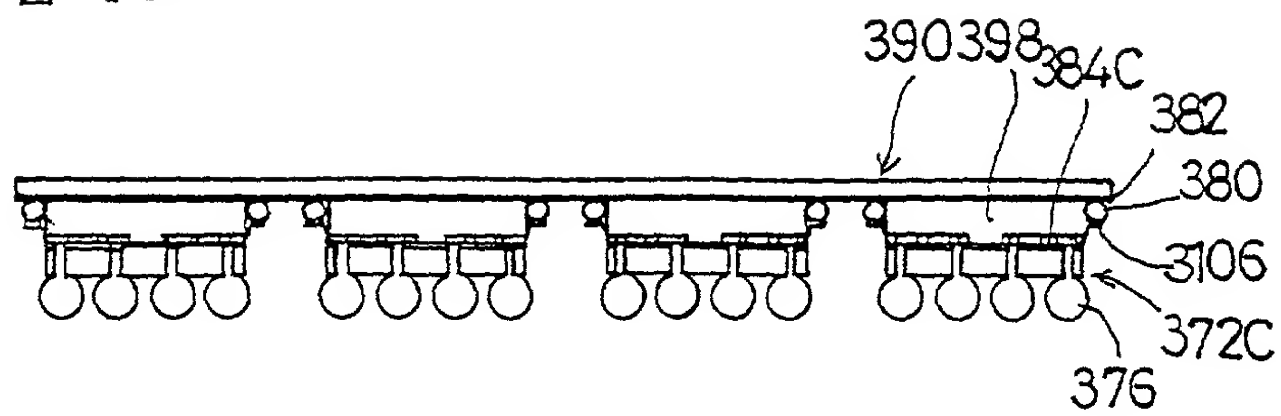


图 169

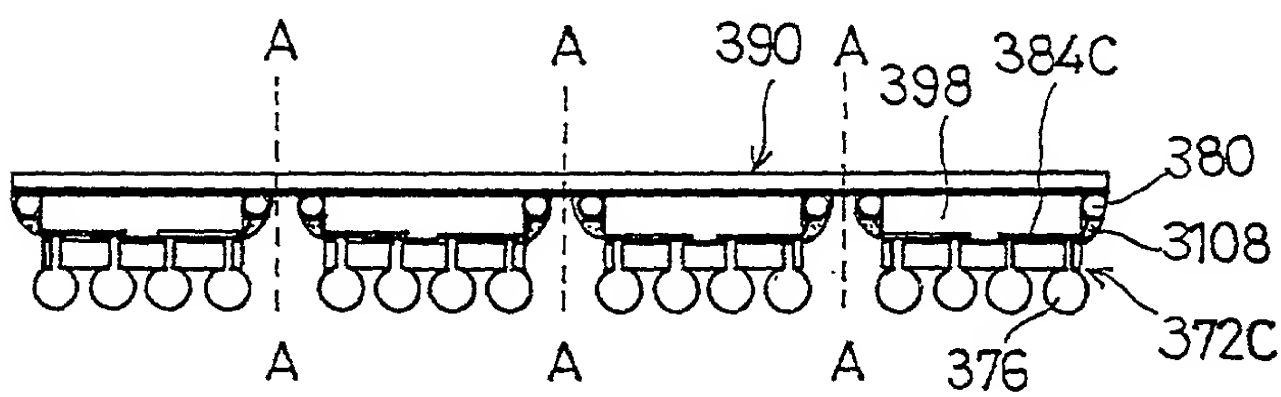


图 170

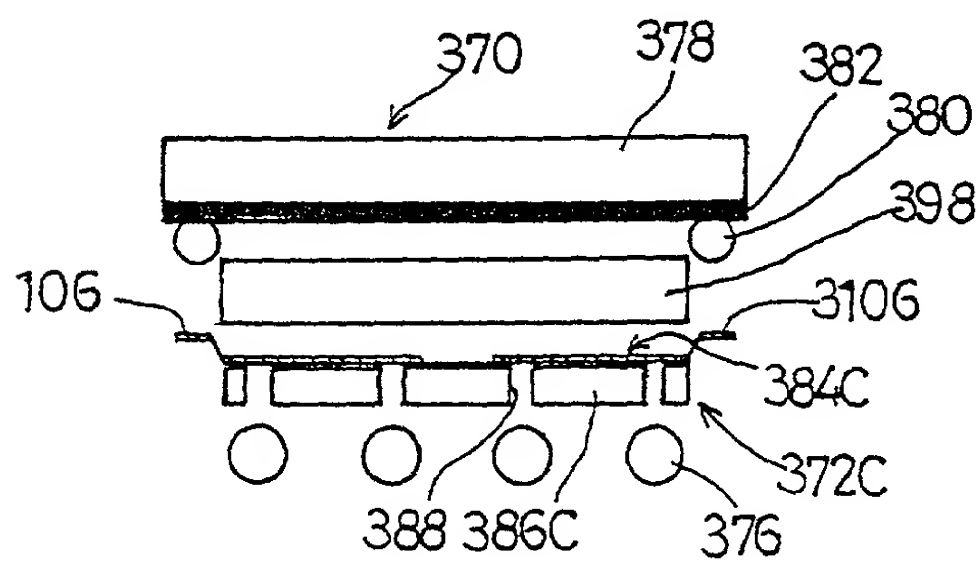


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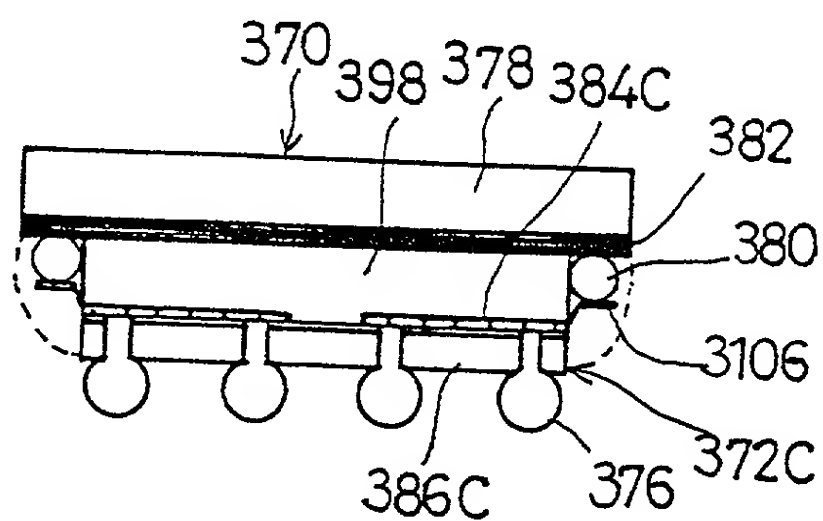
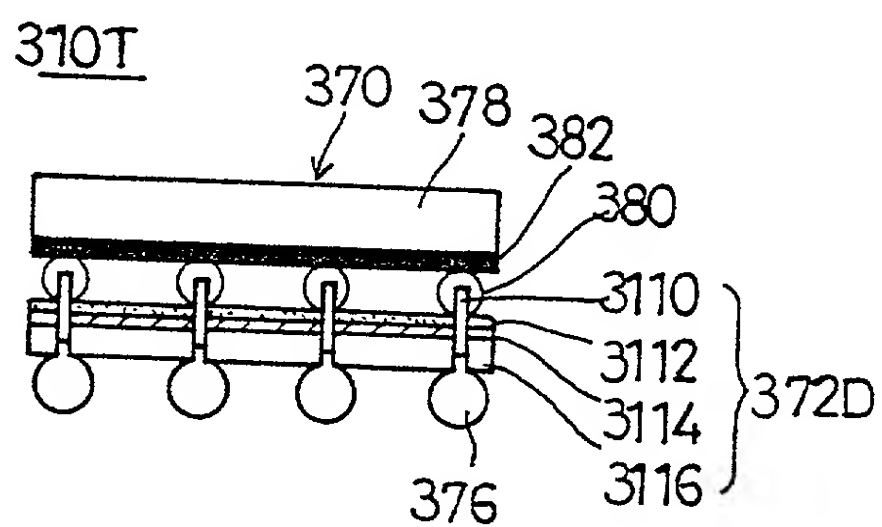
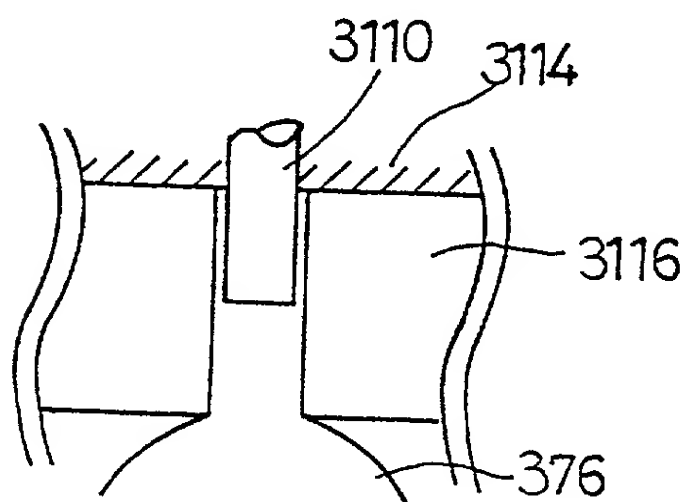


図 172

(A)

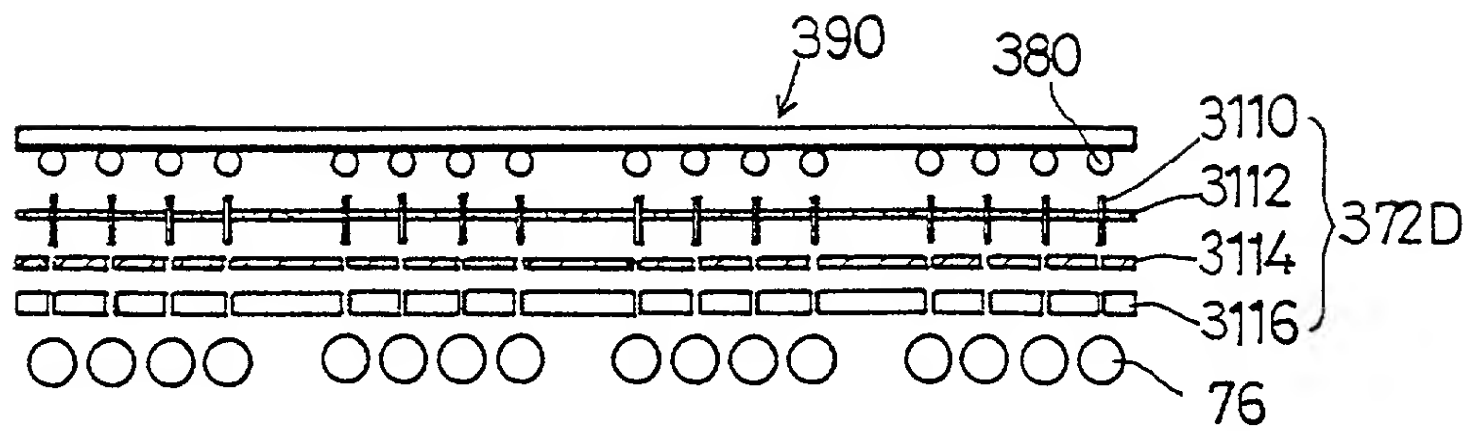


(B)

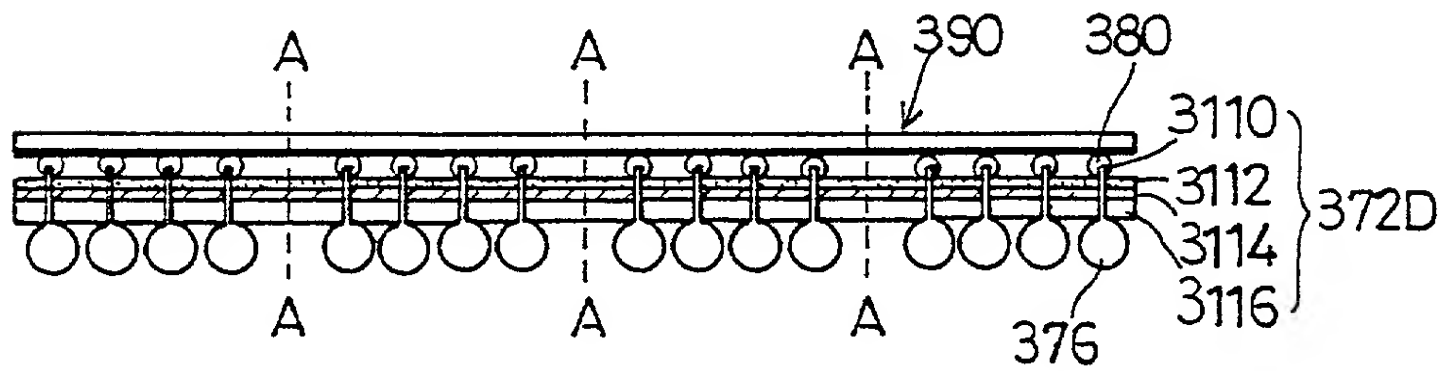


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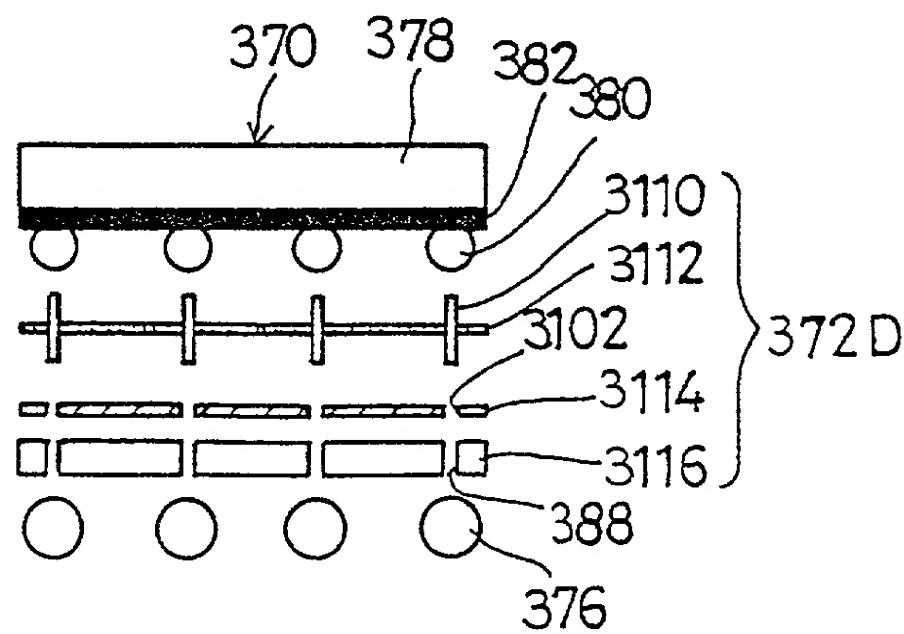


図 176

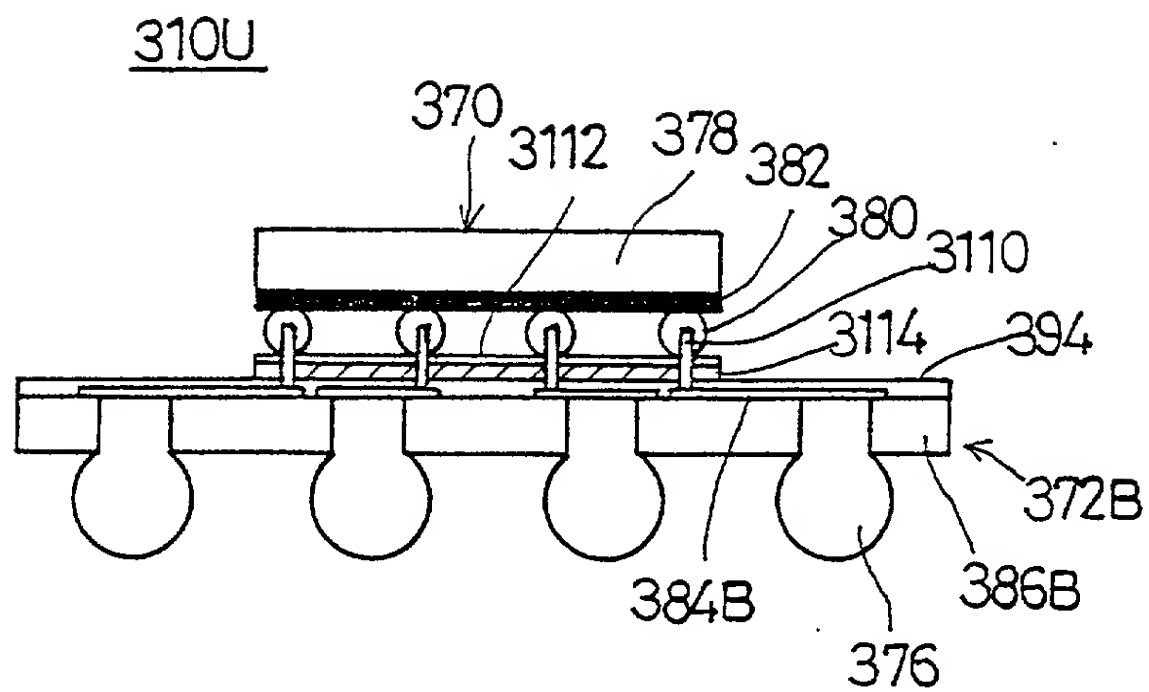


図 177

